Semiconductor-on-Polymer Wafer Level Chip Scale Packaging

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Abstract

IC packages are getting thinner to facilitate thinner devices. Labels and tags are getting smarter. Electronics are starting to bend, and reliability is in question. Semiconductor-on-Polymer (SoP) Chip Scale Packaging (CSP) is enabling ultra-thin flexible hybrid electronics and sensors today. This presentation shares the development of SoP CSP direct interconnect (DI) assembly that has progressed from 24-pin attachment to System-on-Chip assembly of DI pitch at ≤100um in flexible hybrid electronics. Chip Scale Packaging (CSP) defines the logical end of IC package scaling in the package surface area (2D) as package area and IC size converge, for example in direct chip attach (DCA) applications. Scaling thickness is a key metric in packaging evolution. Die thickness is a key contributor to DCA and FC-BGA IC package thickness. SoP can be extended to IC packaging, by facilitating package thickness reduction and improved reliability for CSP/DCA and FC-BGA packages. The presentation also shows the technology roadmap for SoP application to IC packaging.

Key words

Chip-scale-package, CSP, Wafer scale, Semiconductor-on-Polymer, SoP, Ultra-thin

I. Introduction

IC packages are getting thinner to facilitate thinner devices. Labels and tags are getting smarter. Electronics are starting to bend. Consumers think thin is cool. Scaling thickness has, and continues to be, a key metric in packaging evolution. Chip Scale Packaging (CSP) defines the logical end of package scaling in the case of bare die, with Direct Chip Attach (DCA) being the 2D (x-y axis) limit for IC packaging. Die thickness reduction addresses the IC package z-axis for DCA and FC-BGA to the smallest packages possible. Technology and reliability advances in ultra-thin Semiconductor-on-Polymer (SoP) CSP and direct interconnect assembly are enabling flexible hybrid electronics and sensors today. Semiconductor-on-Polymer (SoP) DCA results in ultra-thin semiconductor materials that are less than the thickness possible with bare die. SoP was initially introduced to the flexible electronics market, but now the technology has gained interest for conventional IC packaging. The initial area of interest is low profile, low-mid I/O, DCA type applications. Advanced SoP DCA is an ultra-thin packaging technology that is capable of complete die encapsulation using wafer level processing. SoP can also be applied to higher I/O devices in FC-BGA packages for thinner z-axis profiles.

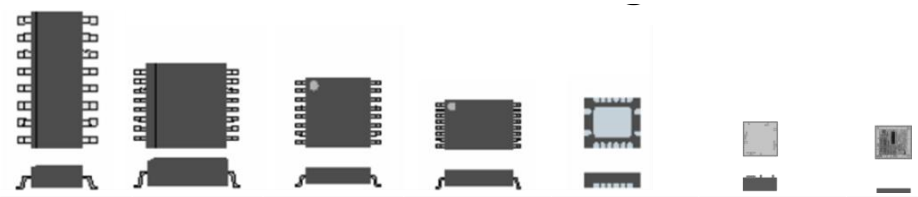
II. Semiconductor-on-Polymer (SoP)

Technology and reliability advances in ultra-thin Semiconductor-on-Polymer (SoP) CSP and direct interconnect assembly is enabling flexible hybrid electronics and sensors today. In the past, CSP's have been defined as a package that is 1.2X the size of the die [1]. However, some types of CSPs maintain their package size as the internal silicon die reduces in size as a result of the fabrication lithography process gets smaller (die shrink). This effect changes the package to die size ratio. As CSP's have evolved, the definition has changed to “near die size” packages with a ball pitch of 1mm or less. SoP extends DCA package volume reduction.

Bare die start losing their mechanical integrity as they are thinned. Ultra-thin bare die for commercial applications are generally limited to no less than 75um in thickness [2]. At thicknesses below 20um they become too fragile to reasonably handle for DCA and eventually unable to maintain functionality unless reinforced. Ultra-thin applications like chip stacking and 3-D integration are current examples of ultra-thin die reinforcement. In SoP CSP, ultra-thin die down to silicon thicknesses of 0.2um

have been demonstrated as robust for SMT and are capable of being handled and assembled in DCA. Major features of SoP CSP include extreme die thickness scaling and improved reliability. Package thickness scaling has reduced to ~1.0mm [3]. Further reduction in thickness has been demonstrated with direct chip attach at 0.075mm (75um), but with the loss of package encapsulation. SoP has been shown to reduce total package thickness to less than 0.030mm (30um) and include full encapsulation using polyimide materials. Device packaging thickness scaling is shown in Fig. 1.

Ultra-thin SoP CSP, shown in the cross-section of Fig. 2, implements full die encapsulation using materials such as polyimides to maintain robust mechanical integrity for ultra-thin semiconductors and interconnects while adding a protective exterior coating to the chip [4]. SoP CSP devices are often sold under the trade name of FleX™-ICs. Silicon and interconnect layers at this thickness, when encapsulated in polyimide, have been demonstrated to achieve radius of curvature (RoC) of less than 5mm without failure. Fig. 2 illustrates that total CSP thickness is typically 30um or less. The wafer level process is capable of sidewall protection without the need for reconstitution during processing. Wafer level processing is less complex and likely lower cost than competing thin die protection processes such as edge encapsulation (CSP area that is greater than die area) and DBF (die backside film) for die backside protection.



Attribute	SOIC-16 (D) [1]	SSOP-16 (DB) [1]	TSSOP-16 (PW) [1]	TVSOP-16 (DGV) [1]	QFN-16 (RGY) [1]	Direct Chip Attach (DCA)[2]	FleX-SoP (SoP) [3]
Length, mm	9.90 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	4.00 ±0.15	2.51	2.163±0.01
Width, mm	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15	2.51	2.283±0.01
Height, Max. mm	1.75	2.00	1.20	1.20	1.00	.075	0.025
Pitch, mm	1.27	0.65	0.65	0.40	0.50	RDL	<0.1
Footprint, mm^2	59.40	48.36	32.00	23.04	14.00	6.3	4.94
Encapsulated	Yes	Yes	Yes	Yes	Yes	No	Yes (PI)
Weight, g	0.150	0.140	0.062	0.040	0.036	~.0008	.00023
SoP area save, %	91.6	89.8	84.6	78.6	64.7	NA	-

Fig. 1. SoP CSP Provides Device thickness Scaling Beyond What is Possible with Bare Die [3]

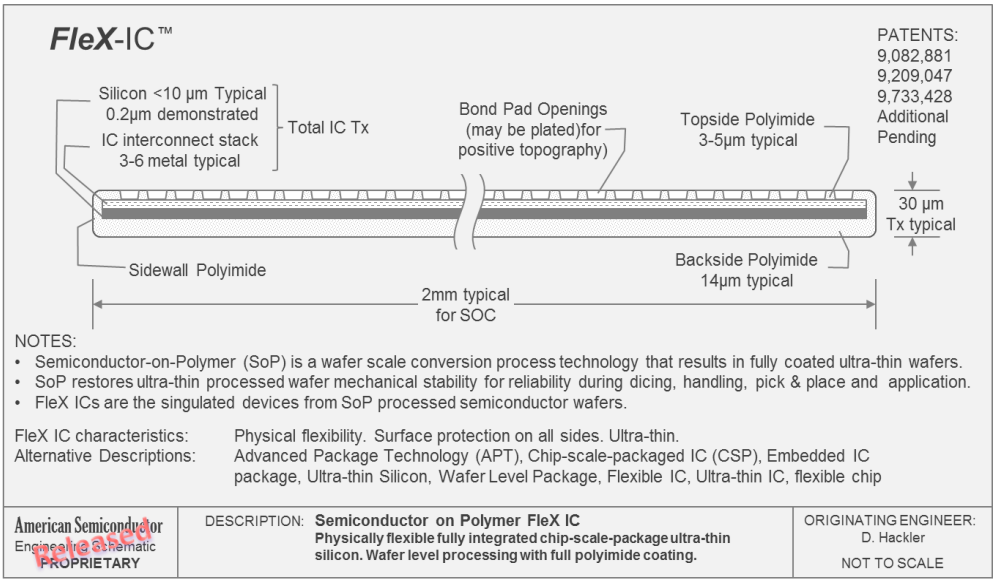


Fig. 2. FleX Semiconductor-on-Polymer Chip Scale Packaging With Sidewall Protection

SoP CSP has been applied to fully characterized commercial devices, uses well-known semiconductor materials, and is generally "qualified by similarity" (QBS). Qualification for flexible applications supplement QBS with test procedures derived from established standards. The initial development of test methods and procedures was done with Air Force Research Laboratory (AFRL) support in 2017. Initial reliability tests augmented with requirements for physical deformation of flexible hybrid electronics (FHE) are described in Table I. SoP CSP is undergoing further characterization for conventional applications. This includes testing that is typical of non-hermetic fully encapsulated parts (Table II).

Flip-chip is the preferred method for assembly of SoP CSP. The ultra-thin package technology feature is fully utilized using Direct Interconnect (DI). Direct interconnect is defined as the die pad interconnect technology where the pad is connected directly to a board pad of equivalent size and spacing. Direct interconnect is common for low pad count devices such as RFID, NFC and other DCA applications. Direct interconnect is not typically considered for higher pin count devices…until now. SoP CSP DI assembly has progressed from 24-pin attachment to System-on-Chip assembly of DI pitch at ≤100um [5]. The technology roadmap for SoP CSP evolution is focused today on ICs with I/O counts of 100 or less (Fig. 3).

Table I (a). FHE Reliability Test Procedures

Test	Conditions	ASI Procedure	References
High Temp Life	125°C	ASI TEST008	ISO 10373-1; JESD22-A108
Low Temp Life	-25°C	ASI TEST009	JESD22-A108
ESD	HBM and/or CDM	ASI TEST010	ANSI-ESDA-JEDEC_JS-001 & JS-002
Static Radius of Curvature	Concave/Convex Bend	ASI TEST003	ASTM D522-93a; ISO 10373-1; ISO 7816
Dynamic Radius of Curvature	Concave/Convex Bend	ASI TEST005	ASTM D522-93a; ISO 10373-1; ISO 7816
Axial Torsion	Twist Test	ASI TEST006	ISO 10373-1; ISO 7816
SEM Inspection	Post SoP Conversion	ASI TEST007	MIL-STD-883: M2018
Data Retention	150°C, non-biased	ASI TEST009	JESD22-A117; JESD-A103

Table I (b). Initial FHE Reliability Test Results

Test	Conditions	Results	Notes
High Temp Life	125°C	Pass	168 hours
Low Temp Life	-25°C	Pass	168 hours
ESD	HBM	Pass	4kV
Static Radius of Curvature	Concave/Convex Bend	Pass	1mm radius
Dynamic Radius of Curvature	Concave/Convex Bend	Pass	10,000 cycles at 5mm radius
Axial Torsion	Bend Test	Pass	90,000 cycles at 180° twist
SEM Inspection	Post SoP Conversion	Pass	4 metal CMOS delayering
Data Retention	150C, non-biased	Pass	500 hours

Table II. SoP CSP Tests in Development

Test	Conditions	References
Moisture Sensitivity Level	1) 168hrs 85°C 85% RH 2) 168hrs 85°C 60% RH 3) 192hrs 30°C 60% RH	JESD22-A113
Thermal Cycling	TCB: -55°C to +125°C TCC: -65°C to +150°C	JESD22-A104
Highly Accelerated Stress Test	130°C 85%RH 33.3psi For 96 to 264hr	JESD22-A110E; MIL-STD-883 101C; JESD22-A102

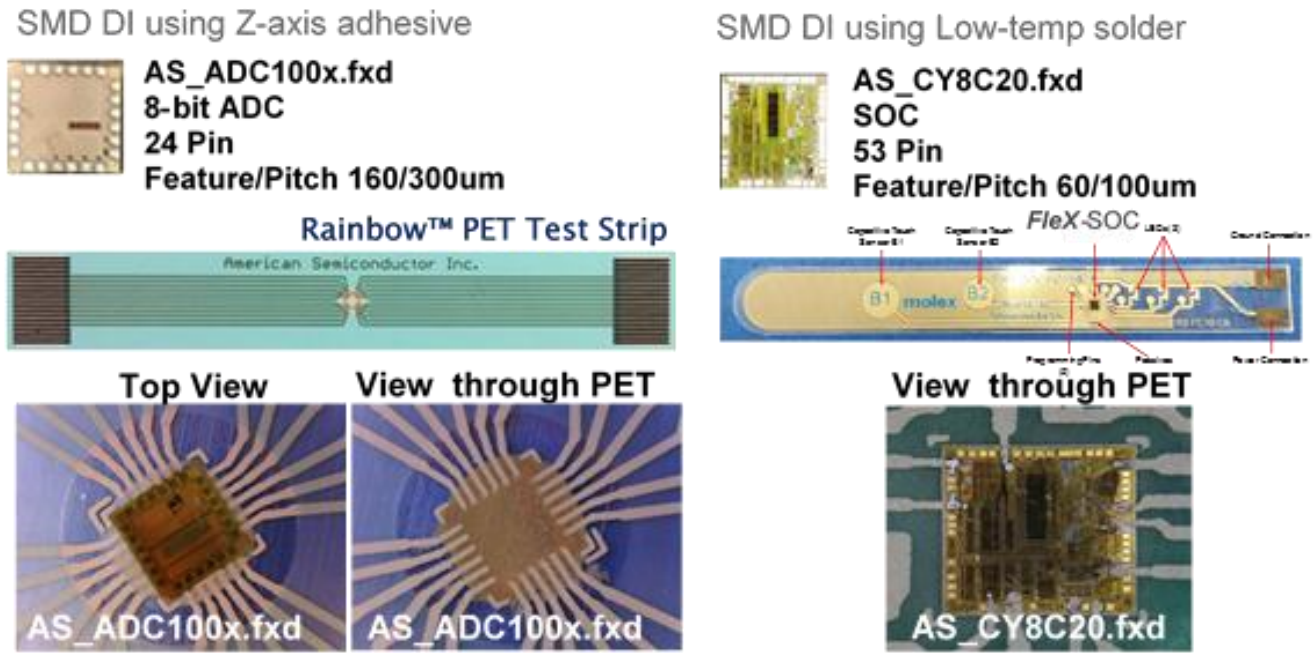


Fig. 3. Scaling of Direct Interconnect (DI) Assembly Progressing to Higher Pin Count Devices

III. SoP CSP Case Study – *FleX*-NFC™

Product labels and data loggers have been demonstrated using SoP CSP. Fully assembled ultra-thin electronic systems based on a FleX-NFC SOC ICs with total thickness of ~35um have resulted in new products that maintain full functionality while being deformed during conformal mounting on curved surfaces and in uses where concave and convex flexing is typical. Labels and loggers based on the new AS_NHS3100P SoP CSP version of NXP's NFC SOC are good examples. This part was the industry's first demonstration of a physically flexible ARM M0+ core with flash memory, temperature sensor and NFC capability. The ultra-thin device was successful assembled on paper, PET and polyimide substrates to create a wide variety of labels and loggers for consumer, beverage and pharmaceutical applications.

IV. Ultra-Thin IC packaging Call to Action

Implementation of ultra-thin IC packaging require demonstration and reliability in actual IC packages for acceptance. System designers that embrace ultra-thin electronics are called to create a vision for putting intelligent electronics into places and things never before possible. Reliability leaders are encouraged to test and model new characteristics of mechanically stressed ultra-thin electronics, to expand test procedures and standards to include physical deformations, to report these results, and to challenge the industry to further improve. Hardware matters – Let's build some new technology.

V. Conclusion

Electronic system requirements are getting thinner. Deformation and bending are natural conditions that must be accommodated in order for future systems to be reliable. SoP CSP has been demonstrated as the thinnest and most reliable capability yet for ICs in ultra-thin and flexible applications. Continued development of the SoP technology roadmap is necessary to fully determine the reliability required, and possible, for new thin electronic systems and for extending SoP capability for high pin count devices.

Acknowledgment

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