This work is sponsored by the Air Force Research Laboratory (AFRL/RVSE)
TPOC: Mr. Kenneth Hebert

45nm Foundry CMOS with Mask-Lite™ Reduced Mask Costs

25 October 2011
DoME
Domestic Manufacturing of Electronics

• Mask-Lite™ 1-D/Grated Layout
  ‣ Reduced Mask Costs
• On-Shore
  ‣ ITAR Compliant
  ‣ TRUSTED Capable
• Economically Feasible for Low Volume
  ‣ DoD
  ‣ Aerospace
  ‣ Commercial
• Supports Process Customization
MRL = Manufacturing Readiness Level  
TRL = Technology Readiness Level 

DoME is a **manufacturing** capability development program

Source: Manufacturing Readiness Levels (MRLs), Jim Morgan, Manufacturing Technology Division AFRL/MLM, Wright-Patterson AFB, 10 May 2006
A 65-nm mask set can cost 1.8 times that of a 90-nm set, while a 45-nm mask set can cost 2.2 times that of a 65-nm set.

- EE Times 10/7/2010
1. AFRL
2. American Semiconductor
   - Process Integration: PDP, FEOL, Cu BEOL, Design...
   - Device Engineering/Modeling – Bill Richards
   - Radiation Hardening – Randall Milanowski
   - ITAR, Trusted in Progress. (Design, Fab and Test)
3. SVTC
   - Fab1 advanced tool set: XT1250 193nm, .85NA
   - Fab2 Cu & 45nm baseline (Sematech ATDF, 2007)
4. Tela-Inc
   - Grated Design & 45nm Commercial Experience
   - 1D Cell Library
5. Silvaco
   - Design Tools
   - PDK and Spice Modeling Support
American Semiconductor
Introduction

CMOS and Custom Semiconductor Foundry

- Corporate Headquarters – Boise, ID
  - Engineering – Design, Process, Modeling
  - Operations/Fab Management
  - Test & Characterization Cleanroom
  - Sales, Marketing, Administration
- Manufacturing – San Jose, CA; Austin, TX (SVTC)
  - Fab/Process Engineering
- Manufacturing – Specialty Process Modules

Privately Held
Founded November, 2001

Product Lines
- FleX™ - Silicon on Polymer
- Design Services – Turnkey Design Solutions

ITAR Compliant; Trusted Certification in Progress
Advanced 45nm CMOS Mask-Lite technology that reduces mask costs up to 90%, making leading edge foundry technology economical for low volume requirements and applications.

Concept
- 1-D straight line geometries
- Non immersion + lower cost reticles
• 1D – geometry
  ‣ Fixed pitch, straight line vs Traditional 2-D with corners
• Enhances Equipment Capability
  ‣ 193nm/.85NA 65nm stepper feasible for 45nm and beyond
• Reduced Mask costs
  ‣ Reduces or eliminates OPC requirements
  ‣ Reduces mask write time, inspection, and repair
  ‣ Dry lithography rather than immersion technology
  ‣ Potential mask reuse from product to product or metal layers (example M1 and M3 masks can be same with different cut masks)
  ‣ E-beam lithography feasibility (Mask elimination)
• Smaller Die
  ‣ Tighter rules allow closer geometries at a feature node or…
  ‣ Same rules with better control for better yield, better timing, better power
- Mask-Lite delivers 77% savings in total MPW wafer lot costs
- Mask costs drive industry multi-project wafer (MPW) lot pricing
- 1-D Mask-Lite technology eliminates major mask cost drivers
  - Eliminates optical proximity correction (OPC)
  - Reduces mask write times, inspection costs, and yield loss

<table>
<thead>
<tr>
<th></th>
<th>Traditional 45nm</th>
<th>Mask-Lite™ 45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>100%</td>
<td>10%</td>
</tr>
<tr>
<td>Poly</td>
<td>100%</td>
<td>10%</td>
</tr>
<tr>
<td>Local Interconnect</td>
<td>100%</td>
<td>10%</td>
</tr>
<tr>
<td>M1-7</td>
<td>7 x 100%</td>
<td>7 x 10%</td>
</tr>
<tr>
<td>Wells, Vt, Strains</td>
<td>10 x 10%</td>
<td>10 x 10%</td>
</tr>
<tr>
<td>NSD, PSD</td>
<td>2 x 20%</td>
<td>2 x 10%</td>
</tr>
<tr>
<td>Pad Metal/Opening</td>
<td>2 x 10%</td>
<td>2 x 10%</td>
</tr>
<tr>
<td>Contacts</td>
<td>2 x 100%</td>
<td>2 x 10%</td>
</tr>
<tr>
<td>Vias (6 layers)</td>
<td>6 x 100%</td>
<td>6 x 10%</td>
</tr>
<tr>
<td>Cuts (4 layers)</td>
<td>N/A</td>
<td>4 x 10%</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>100%</td>
<td>16%</td>
</tr>
<tr>
<td><strong>MULTI-LAYER RETICLE SET</strong></td>
<td>N/A</td>
<td>9%</td>
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</table>
Fast follower strategy leverages industry development of 45nm tools, technology, and know-how to minimize R&D and production costs.

<table>
<thead>
<tr>
<th></th>
<th>DoME</th>
<th>IBM</th>
<th>Intel</th>
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<tbody>
<tr>
<td>Process</td>
<td>ASI AS045BK</td>
<td>IBM Trusted Cu-45HP</td>
<td>Intel 45nm CMOS</td>
</tr>
<tr>
<td>Availability</td>
<td>Pure-play Foundry</td>
<td>IDM/Foundry</td>
<td>IDM</td>
</tr>
<tr>
<td>Mask Cost (tooling)</td>
<td>Low (Mask-Lite™)</td>
<td>Very High</td>
<td>Very High</td>
</tr>
<tr>
<td>Material</td>
<td>Bulk</td>
<td>SOI</td>
<td>Bulk</td>
</tr>
<tr>
<td>Gate (feature/pitch)</td>
<td>45nm/180nm</td>
<td>45nm/190nm</td>
<td>35nm/160nm</td>
</tr>
<tr>
<td>M1 (feature/pitch)</td>
<td>70nm/140nm</td>
<td>TBD</td>
<td>80nm/160nm</td>
</tr>
<tr>
<td>Local Interconnect</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Ion N/PMOS uA/um</td>
<td>800/600</td>
<td>1000/800</td>
<td>1360/1070</td>
</tr>
<tr>
<td>Gate/GOX EOT</td>
<td>Poly/SiON – HKMG</td>
<td>Poly/SiON</td>
<td>High-k/Met. (HKMG)</td>
</tr>
<tr>
<td>Strain</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Lithography</td>
<td>193nm/.85NA</td>
<td>193nm/1.35NA</td>
<td>193nm/.93NA</td>
</tr>
<tr>
<td>1D Grated</td>
<td>Yes</td>
<td>In R&amp;D only</td>
<td>Yes</td>
</tr>
<tr>
<td>BEOL</td>
<td>Cu, low-K, 9 layer</td>
<td>Cu, low-K, 11 layer</td>
<td>Cu, low-k, 9 layer</td>
</tr>
</tbody>
</table>
Why DoME Will Be Successful

• DoME is Structured to be Successful
  › Fast follower strategy implements best known practices for 45nm CMOS (proven commercial technologies, equipment, processes, and knowledge)
  › Pure play foundry uses existing fabrication facilities and equipment (enables low costs for development, prototyping, and low volume production)

• Early Success
  › Functional 45nm CMOS transistors
  › Mask-Lite wafers demonstrated geometries beyond program requirements (showed feasibility to 32nm)
  › 45nm features at target pitch generated using Mask-Lite low cost reticles
<table>
<thead>
<tr>
<th>Process Step</th>
<th>Requirement</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Epi Thickness</td>
<td>Radiation tolerance</td>
<td>Integration complete</td>
</tr>
<tr>
<td>2 Shallow Trench Isolation (STI)</td>
<td>Uniformity and Pitch</td>
<td>Integration complete</td>
</tr>
<tr>
<td>3 Poly Sizing</td>
<td>Uniformity and Pitch</td>
<td>Integration complete</td>
</tr>
<tr>
<td>4 Spacer</td>
<td>Thickness and Uniformity</td>
<td>Integration complete</td>
</tr>
<tr>
<td>5 High Voltage Gate Oxide</td>
<td>Thickness and Etchback</td>
<td>Integration complete</td>
</tr>
<tr>
<td>6 Local Interconnect</td>
<td>Pattern &amp; Continuity</td>
<td>Integration complete</td>
</tr>
<tr>
<td>7 Gate Dielectric: SION HKMG</td>
<td>Cox &amp; Leakage</td>
<td>Integration complete</td>
</tr>
<tr>
<td>8 Strain</td>
<td>PMOS Performance</td>
<td>In progress</td>
</tr>
<tr>
<td>9 Copper</td>
<td>Via/Interconnect Size</td>
<td>In progress</td>
</tr>
</tbody>
</table>
200mm Copper Low-k BEOL

- 45nm CMOS (DoME BEOL)
- 90nm CMOS
- 130nm CMOS (Flexfet BEOL)
- 180nm CMOS
- ITAR

**Can be bolted on to any FEOL**

**Process Design Kit**

- Metal sheet resistance data
- Contact/via sheet resistance data
- Layout design rules
- DRC and LVS rule decks
- Parasitic extraction rule deck
- Electromigration current limits
- Antenna rules
- Global and local alignment marks

This is a simplified illustration. Layers can be replicated and stacked as needed to meet customer requirements.
Prototype Partnership Opportunities

- Contact American Semiconductor: Dale Wilson, Rich Chaney or AFRL/RVSE: Ken Hebert

**Dedicated Runs** with Multi Layer Reticles (MLR)

- Your own mask set and dedicated run for less than the cost of traditional 45nm MPWs
- 10mm x 10mm Field
- Suitable for Prototype and Low Volume Production
- ~200 Gross Die Per Wafer (at 10mm x 10mm)
- ~9% Cost of a Traditional SLR 45nm Mask Set

**MPW** 45nm Multi Project Lots

- 1st Silicon Runs, iterative programs, one-off ASIC’s
- 5mm x 5mm Field (typical, 2x2 to 10x10 available)
- Up to 300 die delivered per MPW tile
- <25% of today’s standard 45nm cost
Thank You

This work was supported in part by the Air Force Research Laboratory under the following programs:

- DoME - Domestic Manufacturing of Electronics
- SHARE - Systematic Hierarchical Approach for Radiation Hardened Electronics
- CRADL - Commercial Rad-hard Advanced Digital Library
- ULP09 - Flexfet ULP CMOS Circuits for Space Electronics