45nm Foundry CMOS with Mask-Lite™ Reduced Mask Costs

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American Semiconductor

Introduction

CMOS and Custom Semiconductor Foundry

- Corporate Headquarters – Boise, ID
  - Engineering – Design, Process, Modeling
  - Operations/Fab Management
  - Test & Characterization Cleanroom
  - Sales, Marketing, Administration
- Manufacturing – San Jose, CA; Austin, TX (SVTC)
  - Fab/Process Engineering
- Manufacturing – Specialty Process Modules

Privately Held
Founded November, 2001

Product Lines
- FleX™ - Silicon on Polymer
- Design Services – Turnkey Design Solutions

ITAR Compliant; Trusted Certification in Progress

This work is sponsored by the Air Force Research Laboratory
45nm Solution
On-Shore. Affordable.

DoME
Domestic Manufacturing of Electronics

• Mask-Lite™
  ‣ 1-D/Grated Layout
  ‣ Reduced Mask Costs

• On-Shore
  ‣ ITAR Compliant
  ‣ TRUSTED Feasible

• Economically Viable for Low Volume
  ‣ DoD
  ‣ Aerospace
  ‣ Commercial

• Supports Process Customization
<table>
<thead>
<tr>
<th>Process Step</th>
<th>Requirement</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Epi Thickness</td>
<td>Radiation tolerance</td>
<td>Integration complete</td>
</tr>
<tr>
<td>2 Shallow Trench Isolation (STI)</td>
<td>Uniformity and Pitch</td>
<td>Integration complete</td>
</tr>
<tr>
<td>3 Poly Sizing</td>
<td>Uniformity and Pitch</td>
<td>Integration complete</td>
</tr>
<tr>
<td>4 Spacer</td>
<td>Thickness and Uniformity</td>
<td>Integration complete</td>
</tr>
<tr>
<td>5 High Voltage Gate Oxide</td>
<td>Thickness and Etchback</td>
<td>Integration complete</td>
</tr>
<tr>
<td>6 Local Interconnect</td>
<td>Pattern &amp; Continuity</td>
<td>Integration complete</td>
</tr>
<tr>
<td>7 HKMG Gate Stack</td>
<td>Cox &amp; Leakage</td>
<td>In progress</td>
</tr>
<tr>
<td>8 Strain</td>
<td>PMOS Performance</td>
<td>In progress</td>
</tr>
<tr>
<td>9 Copper</td>
<td>Via/Interconnect Size</td>
<td>In progress</td>
</tr>
</tbody>
</table>
A 65-nm mask set can cost 1.8 times that of a 90-nm set, while a 45-nm mask set can cost 2.2 times that of a 65-nm set.

- EE Times 10/7/2010
The desired shape is in blue. The shape after OPC is applied is in green. The shape in red is how the feature prints on the wafer.


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- EE Times 10/7/2010
Advanced 45nm CMOS Mask-Lite technology that reduces mask costs up to 90%, making leading edge foundry technology economical for low volume requirements and applications.

Concept
- 1-D straight line geometries
- Non immersion + lower cost reticles
1D – geometry
  - Fixed pitch, straight line vs Traditional 2-D with corners

Enhances Equipment Capability
  - 193nm/.85NA 65nm stepper feasible for 45nm and beyond

Reduced Mask costs
  - Reduces or eliminates OPC requirements
  - Reduces mask write time, inspection, and repair
  - Dry lithography rather than immersion technology
  - No double patterning required
  - Potential mask reuse from product to product or metal layers (example M1 and M3 masks can be same with different cut masks)
  - E-beam lithography feasibility (Mask elimination)

Smaller Die
  - Tighter rules allow closer geometries at a feature node or...
  - Same rules with better control for better yield, better timing, better power
Fast follower strategy leverages industry development of 45nm tools, technology, and know-how to minimize R&D and production costs.
Platform-Based Structured ASIC for space applications utilizes:
1. Performance, logic density, and power of 45nm CMOS
2. Low cost user customization through Mask-Lite for low volume applications
3. Rad-hard design techniques
Platform-Based Structured ASIC Advantages and Applications

Advantages
✓ Performance and density similar to a custom ASIC
✓ Lower design and manufacturing costs than a custom ASIC
✓ Cost effective for low to mid volume quick-turn designs
✓ User configuration via standard EDA tools
✓ Fixed microcontroller is implemented with optimized standard cells rather than the structured ASIC logic cells. This provides superior performance and lower power consumption than a typical FPGA-based design.

Applications
• Sensor data handling
• Actuator control
• Data collection, compression, encryption, and transmission
• ASIC prototypes
Your Project in 45nm

DoME is ready for early collaboration
- Your own mask set and dedicated run for less than the cost of traditional 45nm MPWs
- Multi Layer Reticles supported to further reduce mask costs

DoME is available for process customization
- Add custom process modules
- Target unique performance goals
- Supported with custom PDKs
- Process integration and design support
Thank You