High Performance Single Crystal CMOS on Flexible Polymer Substrate

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Abstract: *FleX™ Silicon-on-Polymer is a substrate conversion technology that delivers low cost, high performance SOI CMOS in a flexible format. FleX enables a new generation of durable, pliable ICs that greatly improves the ability to integrate CMOS functionality in flexible electronics. FleX technology combined with Flexfet Advanced CMOS provides an Ultra Low Power solution that further benefits portable and battery powered applications.*

Keywords: FleX; Silicon on Polymer; flexible CMOS; 3D IC; SOI; thin film transistor (TFT); roll-to-roll; substrate transfer technology (STT); Flexfet; Ultra Low Power (ULP); double-gate CMOS

Introduction

Flexible electronics continue to generate interest in both military/aerospace and consumer markets. Flexible displays are an application driving early adoption of flexible form factors. Commercial markets buzz originated with conformal displays and roll-up electronic newspapers. Today's markets include next generation super thin and rugged flexible e-book readers and notepads. Flexible display technology continues to improve to suit different applications. However, high performance electronics for flexible systems have not yet emerged and remain a barrier to creating flexible systems. Key elements such as memory and logic present different challenges to fabricate in a flexible form since they require significantly higher transistor density and much higher performance than displays.

Current solutions for flexible transistors are not suited to delivering the performance and transistor density that advanced ICs require. Thin Film Transistors have been proven in flexible formats but are far too large for the transistor density requirements and have electron mobilities far too low to provide CMOS-like performance. CMOS technologies have the performance required, but require rigid substrates such as standard silicon wafers. Conventional wafer thinning techniques result in fragile die that are not truly flexible.

FleX Silicon-on-Polymer technology addresses the need for high-performance CMOS in a flexible format. FleX is a novel substrate conversion technology enabling circuitry on SOI wafers to be converted to a flexible polymer substrate. The resulting flexible ICs may be used as a traditional IC die, as very large form factor die, or even used on a wafer scale as a flexible wafer. The FleX process was applied to Flexfet SOI CMOS wafers at 180nm and 130nm process nodes to demonstrate mechanical samples of flexible, high performance CMOS in 2009. This year, continued development is demonstrated with functional flexible CMOS circuits.

FleX Process Overview

The bottom portion of an SOI substrate is referred to as the handle silicon. The handle silicon provides mechanical rigidity during wafer processing. Wafers are often thinned before use and the final thickness may depend on process concerns or end use requirements. Current industry practices generally thin to a minimum of 50 microns of handle silicon remaining, yielding a wafer that can be bent but is fragile and not truly flexible.

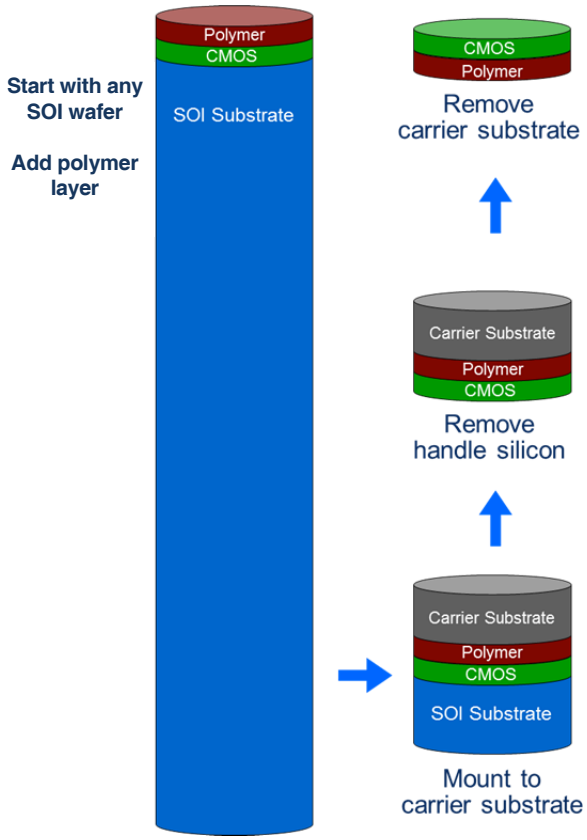

Figure 1. FleX Process Steps.

FleX is unique in that it is not a thinning process but a substrate conversion technology.

The first step in the FleX process is to apply the new polymer substrate to a finished SOI wafer, as shown in Figure 1.

Next a carrier substrate is attached to the polymer side of the wafer. This provides additional mechanical rigidity for the wafer through the next process steps where the handle silicon is completely removed.

At this stage the wafer may receive additional processing to what was originally the backside of the wafer. Bond pads are formed through the original backside of the wafer, but further processing is available.

Finally the finished FleX wafer is removed from the carrier substrate as full flexible wafer. A finished FleX wafer and die are shown in Figure 2. The curl exhibited by the FleX wafer is to demonstrate the flexibility of the Silicon-on-Polymer wafer. The FleX process has a very balanced stress that yields flat wafers.

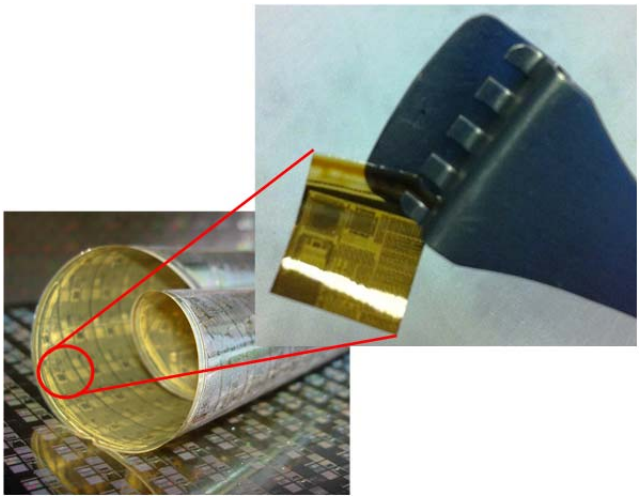

Figure 2. A transparent die and 200mm FleX wafer built on 3 metal Aluminum Flexfet CMOS.

FleX processing can be applied to any SOI wafer. Current production capability is established for 200mm wafers, but other wafer sizes are possible. Results in this paper were achieved using Flexfet™ CMOS fabricated on standard SOI substrates.

Advantages of Flexible CMOS

Flexible CMOS offers several advantages over traditional thick, rigid ICs. The advantages of FleX will vary depending on application specific system requirements, and certain applications may derive benefits not listed here.

Flexibility is the most obvious advantage of FleX. Traditional CMOS is rigid and fragile, which does not work well in flexible systems. FleX delivers ICs on a substrate that is flexible and pliable, allowing CMOS to be conformally mounted on non-flat surfaces or even deformed during operation.

FleX offers durability not seen in traditionally thinned CMOS. Full thickness silicon wafers are approximately 725 microns of silicon substrate. At this thickness the wafers are rigid, but fragile. If dropped, a full thickness wafer will shatter. Full thickness die are sensitive to thermal stress where the handle silicon cracks or shatters. Traditionally thinned die suffer similar limitations. Wafers thinned as low as 50 microns will bend slightly, but are not flexible. These wafers are very fragile, and handling them is a challenge. Thinned die also suffer thermal stress issues, as even 50um of silicon is the majority of the mass in a die. FleX greatly improves on both of these issues. FleX wafers are very mechanically robust. If a full wafer is dropped it gently drifts down with no breakage, similar to dropping a sheet of paper. FleX is flexible. Wafers have been rolled as tight as 20mm, unrolled and tested with no change in electrical results. FleX is more robust with regard to thermal issues as there is practically no silicon remaining in the wafer.

Size is a concern for a wide variety of systems from spacecraft to consumer electronics. Current state of the art for IC space reduction is multi chip packages with several die stacked inside an IC. FleX offers the ability to drastically increase the number of die that may be stacked in a single package, or reducing the height of a package with the same number of die. FleX may also enable new chip stacking techniques that cannot be implemented using traditional thinned die.

Potential Applications

Flexible electronics is an emerging field that is just starting to gain traction. As such, it is impossible for the authors to devise an exhaustive list of applications for FleX, as system designers are certain to find creative uses for the technology. However, a short example list is offered for discussion.

Flexible displays are currently under development and show a clear need for flexible CMOS. Currently only the display itself if flexible, with the logic and memory residing off-board in traditional packaged electronics. FleX CMOS offers a clear method to fabricate flexible memory and logic such that the entire display module can be flexible, adding to the utility and durability of the system.

Many consumer applications would find benefit with FleX. One example would be portable devices such as smartphones / e-book readers / tablet PCs. These devices are likely to remain rigid. However, moving to a flexible display would reduce the likelihood of breaking fragile screens. Incorporating flexible logic and memory would also add to the durability of the device.

3-D Integrated Circuits (3DIC) are an area of industry growth. FleX can be easily bonded in either wafer or die

form, directly to other wafers/die or using interposers to form integrated, compact 3DICs.

FleX Leveraging Emerging Technologies

FleX becomes even more interesting when coupled with new technologies that extend the potential of both. One example is combining FleX with Flexfet™ ULP CMOS. Flexfet ULP is fully-depleted SOI CMOS technology that leverages a double-gated architecture to achieve near ideal subthreshold slope while maintaining performance. Flexfet ULP subthreshold slope is shown in Figure 3. Flexfet ULP is currently offered at the 130nm process node, offering CMOS performance at 0.5V.

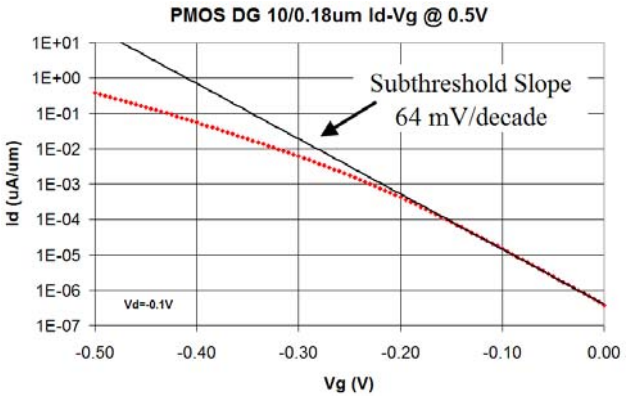

Figure 3. Flexfet ULP near-ideal subthreshold slope

Figure 4 shows a demonstration of Flexfet ULP where a 101-stage ring oscillator is being driven by a parasitic photodiode. This is a fairly crude example, as no special processing was done for the photodiode, which was simply placed near the ring oscillator circuit on the die. The image shows a single microprobe touching a ring oscillator output pad. The ULP ring oscillator is driven completely by scavenged light from ambient artificial room lighting. The ring oscillator frequency is visible in the oscilloscope display in the image. The majority of the power output from the photodiode is being consumed to drive the output. It cannot be shown in the picture, but the frequency of the ring oscillator output was easily varied by increasing the light on the photodiode by using a flashlight, laser pointer, or other auxiliary light source.

Figure 4. Ultra Low Power demonstration of energy scavenging circuits

Flexfet ULP delivers a unique set of benefits to IC and system designers. Ultra low power CMOS directly addresses the size, weight, and power issues (SWaP) facing many applications. By reducing the operating voltage to 0.5V, Flexfet ULP significantly reduces the power requirements of the IC. This drives a reduction in power supply requirements saving both size and weight by requiring smaller batteries, solar arrays, or other power generation/storage devices. As shown in the Figure 4 demonstration, many ICs may even be powered by scavenged energy, completely eliminating power storage and/or generation concerns.

Flexfet ULP combined with FleX enables a new class of mixed-signal circuits for portable, wearable, or space constrained applications.

Technology Status

FleX has been demonstrated on 200mm silicon using substrate transfer technology to create flexible silicon on polymer, showing a feasible path for integration of high performance CMOS for flexible electronics applications. Multiple lots of Flexfet CMOS have run through the FleX process, demonstrating a reproducible process suitable for volume manufacturing. At the time of writing, fabrication of Flexfet ULP wafers through the FleX process is in line, with the expectation of demonstrating the Figure 4 demo on a flexible wafer at GOMAC 2011.

Conclusions

FleX demonstrates a new, flexible, Silicon-on-Polymer technology for low cost, high performance CMOS that meets market expectations for flexible electronics. Combined with Flexfet, FleX technology provides an ultra low-power solution that further benefits portable and battery powered applications.

Acknowledgements

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