A Silicon-on-Insulator Transistor Resistant to Substrate Potential

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***Abstract*—A silicon-on-insulator transistor that is resistant to substrate potential is demonstrated. The 0.18 µm independently double-gated Flexfet™ transistor with implanted JFET bottom gate shows little change in either threshold voltage or leakage current across a wide range of substrate potentials. Threshold voltage shifts (ΔVt) and changes in leakage current for both nMOS and pMOS transistors are analyzed for substrate biases ranging from –20 V to +20 V. Results show no more than 20 mV and 10 mV ΔVt for the nMOS and pMOS transistors, respectively, and leakage currents that change less than 12 pA. The Flexfet™ transistors are therefore ideally suited for applications that require large potentials in the SOI substrates, such as CMOS SOI pixel detectors.**

I. Introduction

In standard SOI processes, the buried oxide (BOX) acts as the dielectric for a parasitic back gate to the transistors. The application of large potentials to the SOI substrate degrades the CMOS transistor performance by changing the threshold voltage (Vt) and increasing the transistor leakage current (Ioff) [1], [2].

The independently double-gated Flexfet™ SOI transistor includes a self-aligned, implanted JFET bottom gate (BG) as illustrated in Fig. 1 [3], [4]. The bottom gate of the Flexfet™ transistor not only provides dynamic adjustment of the threshold voltage, but is also an effective shield against the substrate potential. The Flexfet™ transistors are ideally suited for applications that require large potentials in the SOI substrates, such as CMOS SOI pixel detectors. These pixel detectors can be used for applications such as high-energy particle detectors or photo sensors.

II. Experimental

The Flexfet™ transistors under investigation were fabricated at the 0.18 µm node, with a width of 10.5 µm and a gate length of 0.18 µm. The SiO_2 thicknesses of the gate oxide and buried oxide (BOX) are 35 Å and 1450 Å, respectively. To perform the measurements, a Hewlett-Packard 4156A Semiconductor Parameter Analyzer (SPA) was utilized.

To examine the change in Vt and Ioff, a standard ID-VG test was run at 1.8 V. For the nMOS, the source (VS) was biased at 0.0 V, the drain (VD) at 1.8 V, the top gate swept (VTG) from 0.0 to 1.8 V, and the bottom gate (VBG) stepped -0.5 V, 0.0 V, and 0.5 V. The bottom gate voltage steps were to demonstrate the dynamic Vt capability of the independently double-gated Flexfet™ transistors. The pMOS test was similar with VD = 0.0 V, VS = 1.8 V, VTG swept from 1.8 to 0.0 V and VBG stepped 2.3 V, 1.8 V, and 1.3 V. In both cases the substrate bias (VSUB) ranged from -20 V to +20 V, in 5 V intervals. From the ID-VG measurements at each substrate bias, the threshold voltage was determined and the leakage current was evaluated.

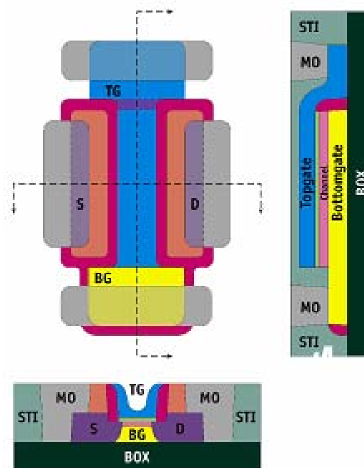

Fig. 1. Flexfet™ cross-section views illustrating the implanted JFET bottom gate (BG) and buried oxide (BOX) layers.

III. Results and Discussion

The experimental results for the nMOS and pMOS devices with the Flexfet™ bottom gates at the same potential as the source are shown in Fig. 2 and 3, respectively. These figures illustrate the transistor ID-VG characteristics as a function of the applied substrate potential. Across the full 40 V range of the substrate potential, the pMOS device shows no more than a ΔVt of 10 mV. The largest ΔVt exhibited by the nMOS device was 20 mV.

Another common problem for SOI transistors with applied substrate bias is an increase in drain-source leakage due to the parasitic back gate transistor. Over the 40 V range of substrate bias, the Flexfet™ transistor leakage (Ioff) variation was only 12 pA for nMOS and 2 pA for PMOS.

In [2], similar tests were run on standard 0.15 µm fully depleted SOI devices. Their results show a ΔVt greater than 0.5 V for both the NMOS and pMOS transistors. Fig. 4 compares the Flexfet™ threshold voltage variation results

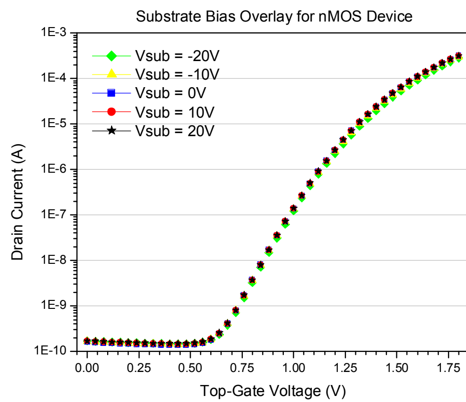

Fig. 2. ID-VG with substrate bias for the nMOS Flexfet™ transistor.

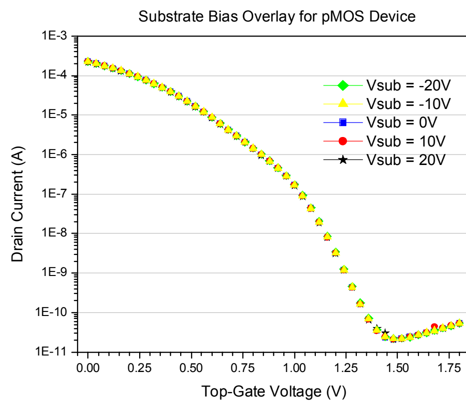

Fig. 3. ID-VG with substrate bias for the pMOS Flexfet™ transistor

with those reported in [2] for their nominal logic transistors. The BOX in [1] is 38% thicker than that of the Flexfet™ devices, 2000 Å versus 1450 Å, and would be expected to provide better resistance against substrate bias effects. Clearly, the Flexfet™ bottom gate prevents substrate-biasing from affecting transistor performance.

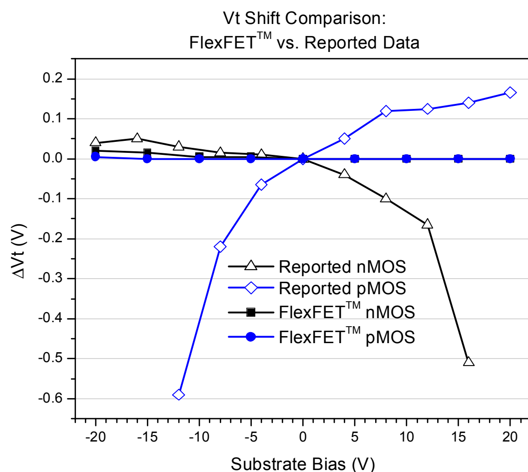

Fig. 4. Measured threshold voltage (Vt) as a function of substrate potential comparing Flexfet™ performance to data reported in [2].

The bottom gate of the Flexfet™ transistors also allows for dynamic threshold voltage adjustment. Fig. 5 and 6 illustrate both the dynamic Vt control and the resistance to the substrate potential. The Vt control provided by the bottom gate is greater than 300 mV and is essentially unaffected by the substrate potential.

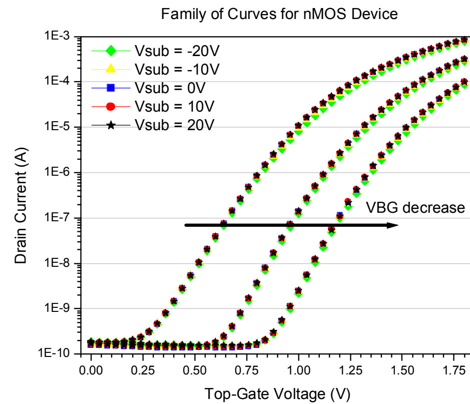

Fig. 5. ID-VG showing dynamic threshold adjustment for the nMOS Flexfet™ transistor

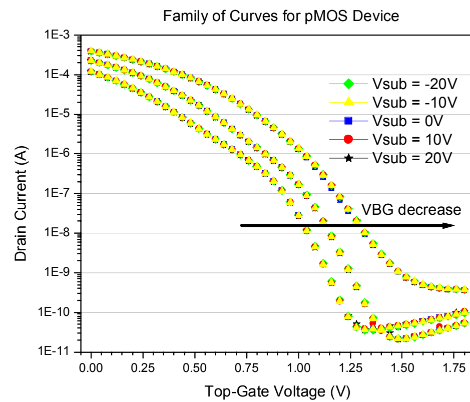

Fig. 6. ID-VG showing dynamic threshold adjustment for the pMOS Flexfet™ transistor

IV. Conclusions

This study investigated the effects of substrate potential on 0.18 µm Flexfet™ SOI transistors. Results show no more than 20 mV of threshold shift and a less than 12 pA change in leakage current. The Flexfet™ bottom gate prevents the substrate bias from degrading transistor performance. In addition, the dynamic threshold voltage adjustment capability of Flexfet™ is similarly unaffected by the substrate potential. This makes Flexfet™ an exemplary candidate for SOI pixel detectors in which substrate biasing is necessary.

References

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[4] US Patents 6919657, 7015547, 7019342, and 7154135.