

# Flexfet™: Independently-Double-Gated SOI Transistor With Variable $V_t$ and 0.5V Operation Achieving Near Ideal Subthreshold Slope

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## Introduction

According to the 2006 ITRS roadmap, supply voltages for logic technologies will remain near 1.0 V down to the 32 nm node in 2012 [1]. This prediction makes the realization of ultra-low voltage, high-performance electronics quite challenging. A key reason for this limitation is the subthreshold slope. Typical subthreshold slopes for bulk CMOS are in the range of 80-90 mV/decade. Flexfet™ in double-gated (DG) mode has demonstrated a near ideal subthreshold slope of 64 mV/decade and in independently-double-gated (IDG) mode provides dynamic  $V_t$  control. Initial demonstration of the device is presented at 180 nm channel lengths. 130 nm channels have been successfully fabricated and scaling has been verified with simulation to beyond the 65 nm node.

Flexfet™ is a planar IDG MOSFET with a damascene metal top gate and an implanted JFET bottom gate that are self-aligned in a gate trench as shown in Fig. 1 [2]. The device can best be understood as a metal-gate fully-depleted SOI MOSFET in parallel with a JFET where both devices share their drain, source, and channel. This device is highly scalable due to its sub-lithographic channel length, non-implanted ultra-shallow source/drain extensions (SDE), non-epi raised SD regions, and gate-last flow.

Most damascene gate processes use a dummy gate and implanted SDE junctions [3-4]. Flexfet™ uses a spacer-lined gate trench etched through implanted SD regions to self-align the implanted JFET bottom gate with its metal top gate. The damascene top gate and diffused SDEs prevent damage to the channel edges. Raised SD regions are achieved without using selective epi.

## Process Description

Only 8 masks and 10 masking steps are required to build Flexfet™ CMOS circuits through M1. The starting material is Unibond 10  $\Omega$ -cm p-type SOI wafers with  $t_{SOI} = 200$  nm. For Flexfet™ NMOS transistors, a shallow N+ phosphorous SD implant is followed by deposition of a 190 nm nitride pad. 300 nm deep isolation and gate trenches are simultaneously etched through the nitride and into the SOI to separate the source from the drain. This is followed by an anneal to partially drive the SD junctions. Next, the bottom gate (BG) mask is used to protect the channel regions while completing the

isolation etch down to the BOX. This is followed by creation of 35 nm oxide/nitride spacers. The spacer-lined gate trench is used to self-align a  $BF_2$  bottom gate implant with a peak concentration of  $>10^{19}/cm^3$  near the BOX interface.

A 4.5 nm thermally grown gate oxide is followed by the deposition of a 70 nm TiN top gate, thereby avoiding the complexities of typical damascene gates. During gate oxidation, the SD junctions are driven to the BOX and the SD extensions are created. Top gate mask and CMP define the gate electrode. The top gate etch also cuts through the channel to expose the bottom gate contact regions. This gate-last process supports future use of high- $k$  gate dielectrics and other metal gates. A SEM photo of Flexfet™ prior to STI deposition and local interconnect formation is shown in Fig. 2.

## Results and Discussion

Fig. 3 shows Id-Vg operation of a Flexfet™ 0.18  $\mu m$  PMOS transistor with the top and bottom gates connected together in DG mode for 0.5 V operation. A near ideal double-gated subthreshold slope of 64 mV/decade is observed and an  $I_{on}/I_{off}$  ratio of  $10^6$  despite the limited 0.5 V voltage range. Fig. 4 shows the 0.5 V Id-Vd curves for the DG PMOS transistor. Performance improvements could be obtained by using a thinner gate oxide to optimize the Flexfet™ transistor for operation only at 0.5 V. Fig. 5 shows a 0.18  $\mu m$  Flexfet™ NMOS transistor operating at 1.8 V in IDG mode. In this figure, the IDG mode dynamic threshold voltage adjustment using the bottom gate is clearly visible. Fig. 6 provides similar data for a PMOS Flexfet™ transistor. The bottom gate provides 0.29 V/V and 0.34 V/V of  $V_t$  adjustment for the NMOS and PMOS transistors, respectively, in IDG mode.

## Conclusion

Manufacture of Flexfet™ CMOS with excellent dynamic threshold control has been demonstrated. Flexfet™ transistors operating at 0.5 V in DG mode have demonstrated a near ideal subthreshold slope of 64 mV/decade and an  $I_{on}/I_{off}$  ratio of  $10^6$ . In IDG mode, the Flexfet™ bottom gate provides a wide range of dynamic  $V_t$  adjustment enabling flexible device configurability for future ultra-low-power designs.

### References

- [1] *Overview and Working Group Summaries*, International Technology Roadmap for Semiconductors: 2006 Update, [www.itrs.net/links/2006Update/FinalToPost/00\\_ExecSum2006Update.pdf](http://www.itrs.net/links/2006Update/FinalToPost/00_ExecSum2006Update.pdf)
- [2] US Patents 6919657, 7015547, 7019342, and 7154135.
- [3] K. Matsuo, et. al., *High Performance Damascene Gate CMOSFETs with Recessed Channel Formed by Plasma Oxidation and Etching Method*, IEDM Tech. Dig., pp. 445-448, Dec. 2002.
- [4] F. Cornu-Frueux, et. al., *Spacer-First Damascene-Gate FinFET Architecture Featuring Stringer-Free Integration*, IEEE Electron Device Letters, Vol. 28, No. 6, pp. 523-526, June 2007.

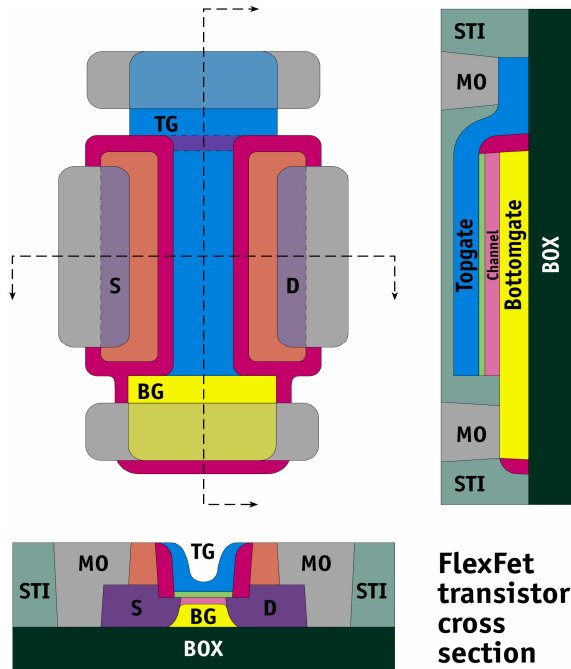


Figure 1. Flexfet™ top view and cross-sections

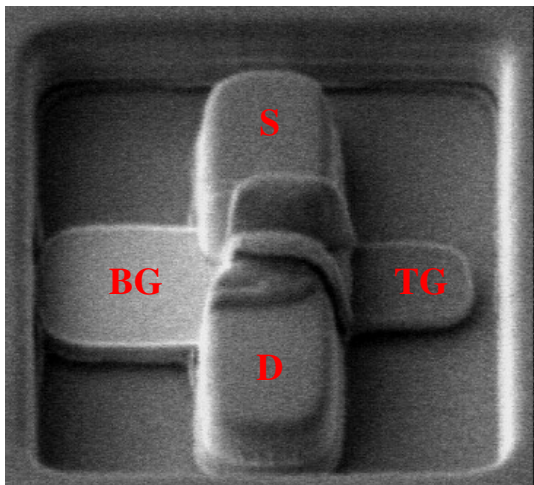


Figure 2. SEM photo of single Flexfet™ 0.18µm independently-double-gated MOSFET

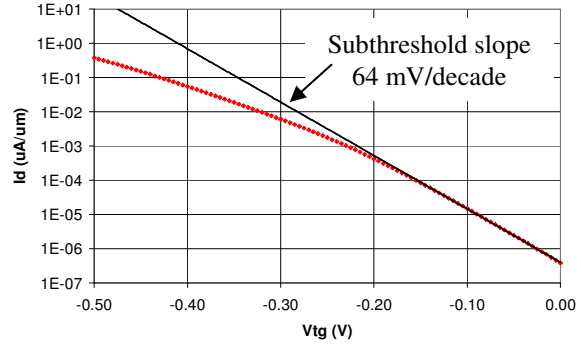


Figure 3. Flexfet™ 0.18 µm PMOS Id-Vg operating in double-gated (DG) mode with Vd=-0.1 V

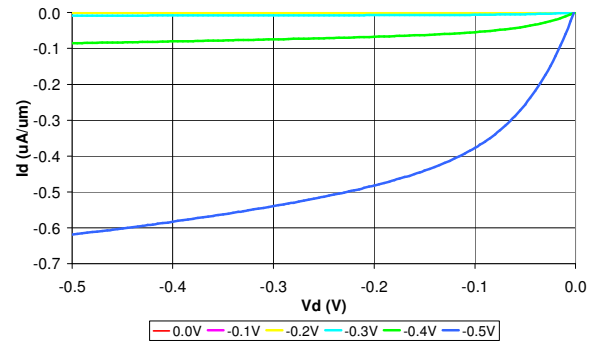


Figure 4. Flexfet™ 0.18µm PMOS Id-Vd operating in double-gated (DG) mode for 0.5 V operation

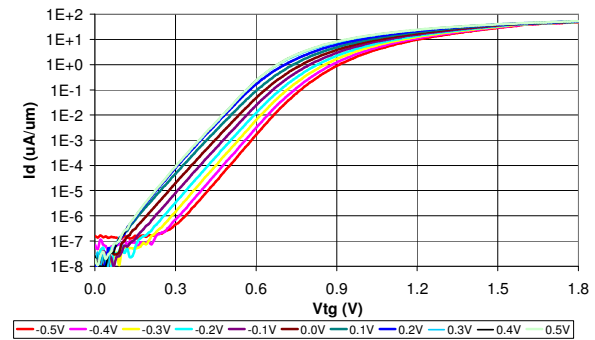


Figure 5. Flexfet™ 0.18 µm NMOS Id-Vtg as a function of Vbg with Vd=0.1 V in IDG mode

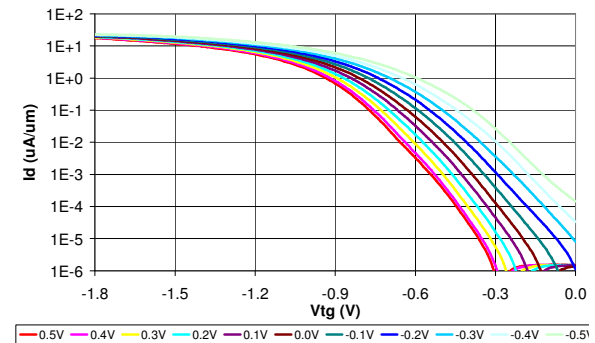


Figure 6. Flexfet™ 0.18 µm PMOS Id-Vtg as a function of Vbg with Vd=-0.1 V in IDG mode