

Rad-Hard Reconfigurable Bi-Directional Level Shifter (ReBiLS) for NASA Space Applications in the Flexfet™ 0.18 μm SOI CMOS Technology

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Abstract—There are different chip I/O voltages available for space system designer use ranging from 0.5 V to 5.0 V. Rad-hard reconfigurable bi-directional level shifters (ReBiLS) provide NASA spacecraft designers with a solution to interface various voltage level chips with each other. ReBiLS can integrate existing space systems with ultra-low power (ULP) chips. The ReBiLS design translates 0.5 V logic bi-directionally to 1.2 V, 1.8 V, and 2.5 V at frequencies up to 500 MHz. The radiation tolerant capability of the ReBiLS design is derived from the Flexfet™ technology which has demonstrated total ionizing dose (TID) tolerance in excess of 1Mrad. Control of the bottom gate voltages allows re-configuration to tradeoff power consumption and operating speed. ReBiLS designs that support voltage translation to 3.3 V and 5.0 V can be achieved with process and circuit modification. American Semiconductor is working in close collaboration with NASA Goddard Space Flight Center and the Center for Advanced Microelectronics and Biomolecular Research (CAMBR).

I. INTRODUCTION

The many different types of integrated circuit technologies available to space system designers often operate at different voltage levels. When building complete systems there exists a common problem of mixing old and new parts operating at incompatible voltages [1]. It is important to maintain, update, and interface to these systems. NASA's spacecraft, like those found on the Space Technology 5 (ST5) project, utilize components that employ a variety of voltage levels including CMOS Ultra-Low Power Radiation Tolerant (CULPRiT) Logic [2].

Additionally, spacecraft have limited supply voltages and power at their disposal [3]. Thus the trend is for newer equipment to use semiconductor technologies that operate at ever lower voltages. Typical flight board designs for NASA spacecraft involve the integration of ICs with I/O voltage levels of 5.0, 3.3, 2.5, 1.8, 1.2, and even 0.5 V parts, such as the ST5 mission's CULPRiT Reed-Solomon encoder from Idaho's Center for Advanced Microelectronics and Biomolecular Research (CAMBR) center.

The Reconfigurable Bi-Directional Level Shifter (ReBiLS) presents a new opportunity for helping the National

Aeronautics and Space Administration (NASA) meet its space exploration needs. ReBiLS may also be used by Air Force Research Laboratory (AFRL), Military Satellite Communication (MILSATCOM), and any other military or commercial entities interested in expanding the design capability of current spacecraft, satellites, and any other form of space vehicles.

Currently, radiation tolerant level shifters are not a commonly available component for space integrated circuit (IC) designers. Systems currently are required to be designed specifically for each implementation. This means that a new level shifter design may be required to complete the integration of two systems. Another challenge for level shifters is the ability to communicate logic levels in both directions for each system the level shifter links together. These issues lead to the need for a level shifter that is universal, radiation tolerant, reconfigurable and bi-directional.

American Semiconductor, Inc. (ASI) directly addressed this NASA need in our recently initiated SBIR project. ReBiLS was designed for fabrication in our advanced 180nm Flexfet™ SOI CMOS on-shore foundry facility at the Cypress Semiconductor Silicon Valley Technology Center (SVTC) in San Jose, CA. Simulations for ReBiLS stand-alone and embedded cells were successfully demonstrated using ASI's advanced double gate Flexfet™ CMOS models during the Phase I effort.

A lower power, higher performance solution for future ultra low power (ULP) NASA spacecraft can be obtained by (1) porting the existing radiation hardening-by-design (RHBD) 0.5 V CULPRiT designs to the more advanced, scalable, inherently radiation tolerant Flexfet™ CMOS process and (2) integrating the 0.5 V to 5.0 V I/O level shifting directly onto the CULPRiT chip. Ultimately the only way to get a true ULP payoff is to design entire ULP boards and systems. A stand-alone ULP chip, such as the telemetry channel coder, which has to drive higher I/O voltages on the board serves as a demonstration of the technology without realizing the full ULP payoff since the high voltage I/O power consumed on the board overwhelms the ULP chip power savings. This project enables the design of ULP flight boards for future NASA exploration missions.

During Phase I of the SBIR project, ASI demonstrated the feasibility of producing a radiation tolerant reconfigurable bi-directional level shifter design. This design utilized ASI's

state-of-the-art, low power, low cost, Flexfet™ process that contains inherent radiation tolerant and sub-lithographic silicon on insulator (SOI) design benefits [4]. Phase I has shown feasibility of level shifter circuits with total dose capability of 1 Mrad, have no latch up concerns, support voltages as low as 0.5 V and as high as 5.0 V, have low power consumption, operate with input/output data rates up to 500 Mb/s, are low cost, and can be easily integrated with multiple systems.

II. FLEXFET™ SOI CMOS TECHNOLOGY

A. Flexfet™ Transistor

The patented Flexfet™ transistor structure can best be understood as a metal-gate accumulation mode MOSFET in parallel with a self-aligned JFET as illustrated in Figure 1. Flexfet™ is a new SOI independently double-gated CMOS technology that features a gate trench etched through thick source/drain regions into which an implanted JFET bottom gate and mid-gap TiN MOS top gate are self-aligned. The independent top and bottom gates are contacted at opposite sides of the channel by a damascene tungsten local interconnect that is embedded in the isolation region between transistors. This results in compact, planar connections to all four transistor terminals. Simplified 2-dimensional device cross sections across both the length and the width of a Flexfet™ transistor are illustrated in Figure 2. Figure 3 shows similar 3-dimensional views of a Flexfet™ transistor.

Individual transistors can be connected as single-gate, double-gate, or independently double-gated, as desired. The single-gate and independently double-gated types can operate to a maximum VDD of 2.5 V in the base Flexfet™ 180 nm process. Double-gate operation is limited to a VDD of 0.8 V.

The Flexfet™ transistor provides the opportunity to use the bottom gate for dynamic reconfigurability for ultra-low-power operation and in-space reconfiguration [5]. This feature may also be used to continuously compensate for TID effects, as well as other wearout effects such as hot-carrier degradation. Therefore, this technology permits the design of dynamically self-repairing circuits, which are tolerant of large total doses of radiation and single event effects (SEE). The Flexfet™ technology is promising for advanced system-on-chip (SOC) solutions for space and missile applications operating in extreme radiation and temperature environments.

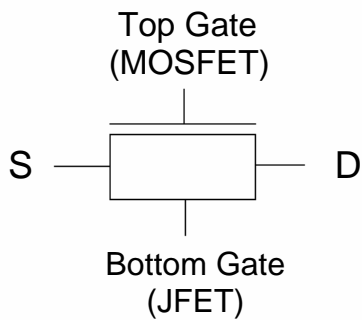
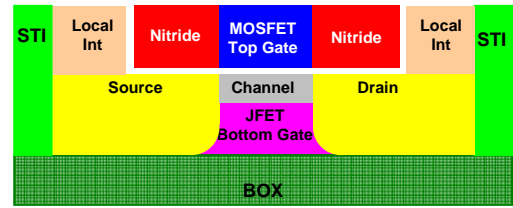
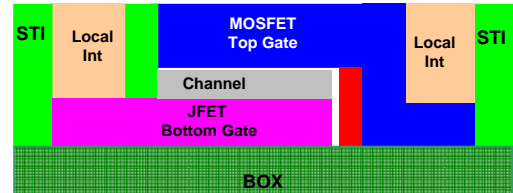


Figure 1. Flexfet™ schematic representation

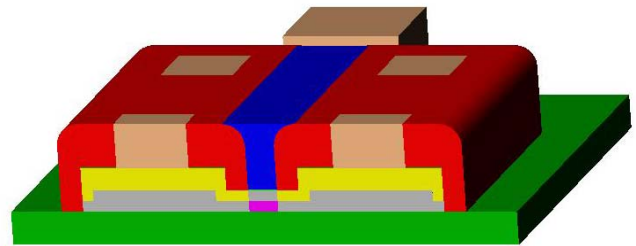


(a) Length cross section

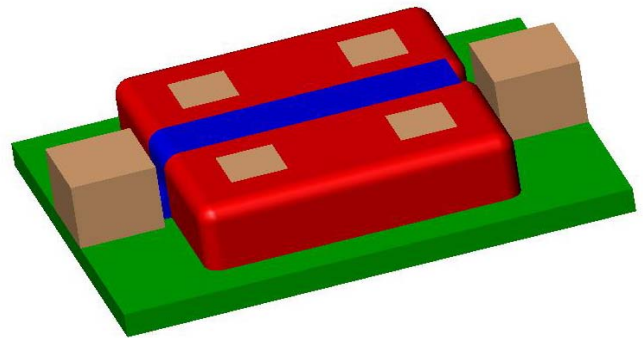


(b) Width cross section

Figure 2. Flexfet™ transistor cross sections.



(a) 3-D length cross section



(b) 3-D top view

Figure 3. 3-D views with shallow trench isolation (STI) oxide removed

B. Flexfet™ Process Overview

Flexfet™ is a low cost, near-fully-depleted SOI process that is inherently total ionizing dose (TID) radiation tolerant in excess of 1 Mrad (as tested at AFRL). Less than one decade of source-drain off-state leakage current increase is observed up to a 1.5 Mrad dose, validating the TID effectiveness of Flexfet™ with resolution of the back channel SOI TID problem.

The Flexfet™ process uses a relatively thick 200 nm SOI layer into which the source/drains are implanted. Gate trenches are then etched through the source/drains. The channel thickness is set by the energy of the bottom gate implant into the bottom of the gate trench, not by the SOI thickness. A raised source/drain structure is achieved without any epi growth thermal budget. Flexfet™ is a gate-last process, allowing high-K or ferroelectric gate dielectrics and metal top gates to be deposited and planarized into the gate trench, thus avoiding any damaging plasma gate etches or subsequent high-temperature processing.

Ultra shallow source/drain extensions are formed by disposable doped glass sidewall spacers. These nitride spacers permit 180 nm channels to be created with relaxed 350 nm lithography [6]. A 4.5 nm gate oxide and a 30 nm TiN layer form the top gate stack. Figure 4 is an SEM view of a Flexfet™ transistor before STI oxide deposition. Only 8 masks are used through Metal 1 for low manufacturing costs. The recessed channel and bottom gate structure maintain an ultra-thin 20 nm channel while allowing 200 nm thick source/drains for lower series resistance. These unique device structural features make the Flexfet™ transistor highly scalable.

Flexfet™ technology is currently beginning 200 mm CMOS production at SVTC with initial customer silicon delivery scheduled for Q4 2005 using the AS180FFc 180 nm version of the process. Table I provides basic process information and performance parameters for the Flexfet™ AS180FFc process.

The technology is forecast to achieve radiation tolerant SEE reliability performance improvement consistent with the TID improvement already demonstrated. The technology features designed to provide SEE performance include reduced transistor silicon volume, the reduction of critical junction cross-section and the improvement of critical charge ratios.

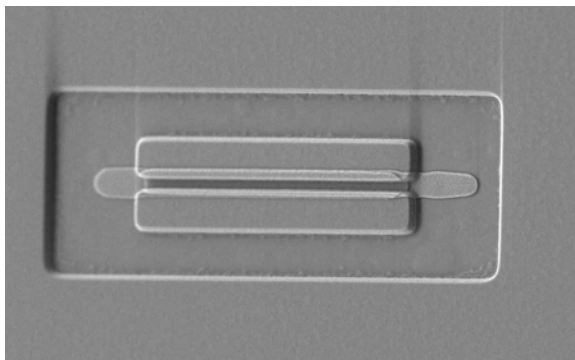


Figure 4. SEM view of Flexfet™ before STI oxide

TABLE I
FLEXFET™ PROCESS INFORMATION AND PERFORMANCE PARAMETERS

Parameter	Unit	AS180FF	
Litho Min Feature	nm	350	
Lmin (physical)	nm	180	
Leff	nm	120	
Tox	Å	50	
Vdd	V	0.5 – 2.5	
Cgate	ff/μm ²	1.1	
Cov	ff/μm	0.24	
PDP = Ctot * Vdd ²	fJ/μm	0.67 (@ 0.5 V) / 14.6 (@ 2.5 V)	
Bottom Gate Vt Control		Vbgate = -0.5 V	Vbgate = 0.5 V
Vt	V	1.0	0.0
Ion (NMOS)	mA/μm	500	900
t = (Ctot * Vdd) / Ion	ps	13.5	4.5
Ioff	A/μm	1.0E-15	1.0E-06
Pstandby = Vdd * Ioff	W/μm	2.5E-15	2.5E-06

III. REBILS DESIGN AND OPERATION

A. Level Shifters Background

Level shifter designs employ circuits that communicate logic signals between different voltage level operating systems as illustrated in Figure 5. These systems can operate at voltage baselines varying from 5.0 V all the way down to 0.5 V. However, individual systems cover only subsets of these voltage ranges. Traditional level shifters only communicate in one direction, i.e. only allowing the flow of data in one direction. In Figure 5 the ReBiLS level shifter is shown to be bi-directional (allowing data flow in to and out from both the low-voltage and high-voltage integrated circuits) with direction control provided by the DIR signal. The BG (bottom gate) control signal(s) are used for speed and power control of the Flexfet™ transistors. Both the low-voltage supply (VDDL) and high-voltage supply (VDDH) are employed by the level shifter.

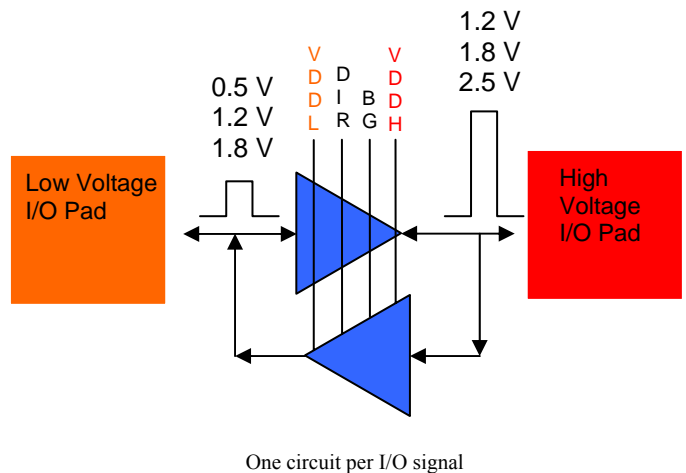


Figure 5. Block diagram of ReBiLS operation

B. ReBiLS Circuit Design

The ReBiLS design is based upon two chains of inverters as illustrated in Figure 6. One chain performs the down-shifting and the other chain performs the up-shifting. Portions

of the circuit operate at the low-voltage supply (VL) and the remainder operates at the high-voltage supply (VH). The devices are sized appropriately to support the required logic level transitions and support fairly wide variation in both the low-voltage and high-voltage supplies. The complementary direction control signals (EN and ENN) select either up-shifting or down-shifting operation and disable any unused circuitry to minimize power consumption. The ability to reconfigure ReBiLS operating performance is provided by the Flexfet™ bottom gate control signals (Vpbg_h, Vpbg_l, and V_{nbg}).

The ReBiLS design of Figure 6 satisfies the requirements for a radiation tolerant, reconfigurable, bi-directional level shifter. When manufactured in American Semiconductor's standard 180 nm Flexfet™ process, the operating characteristics for this ReBiLS design include:

- 1) Multi-level bi-directional operation for 0.5 V ↔ 1.2 V, 0.5 V ↔ 1.8 V, 0.5 V ↔ 2.5 V, 1.2 V ↔ 1.8 V, 1.2 V ↔ 2.5 V, and 1.8 V ↔ 2.5 V.
- 2) High-speed operation of 100 – 500 MHz.
- 3) TID radiation tolerance in excess of 1 Mrad.
- 4) Reconfigurable using Flexfet™ bottom gate voltage control for speed and power optimization.
- 5) Easy optimization to support either stand-alone or embedded level shifting applications.

Table II provides information on the operating characteristics of the ReBiLS design.

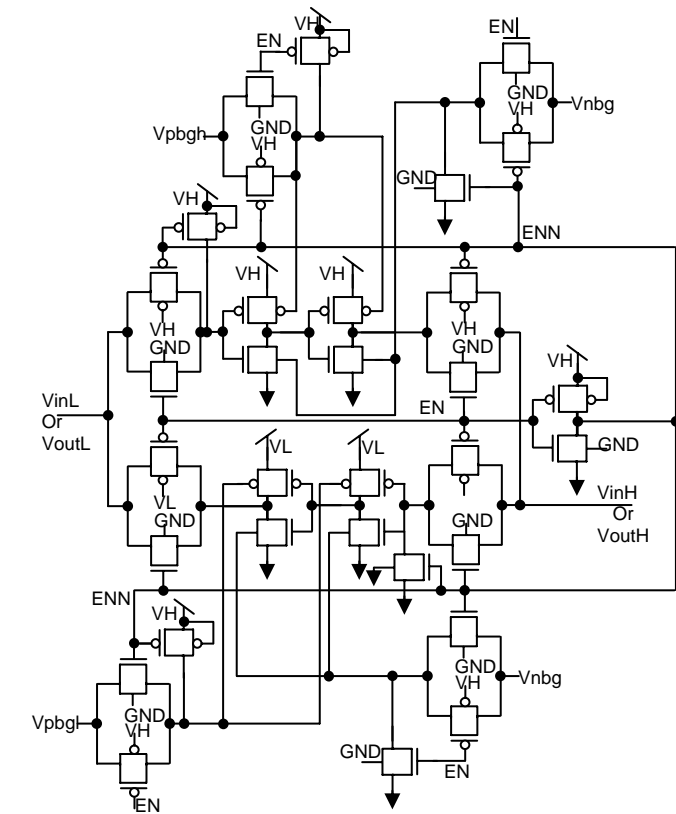


Figure 6. ReBiLS schematic

TABLE II
REBiLS OPERATING CHARACTERISTICS

Parameter	Unit	Min	Max	Typ
VDDH	V	1.2	2.8	2.5
VDDL	V	0.45	1.8	0.5
V _{pbg_h}	V	VDDH - 0.5V	VDDH + 0.5V	VDDH
V _{pbg_l}	V	VDDL - 0.5V	VDDL + 0.5V	VDDL
V _{nbg}	V	- 0.5V	+ 0.5V	0.0V
DIR	V	0.0V	VDDH	0.0V or VDDH
Data rate	MHz	0	500	100
C _{load}	pf	0	20	10
Active power	mW	Depends on operation		10 - 500
Prop delay	ns	Depends on operation		1 - 4
TID tolerance	Mrad	1.0	—	> 1.0

C. ReBiLS Operation

Figure 7 illustrates typical ReBiLS 0.5 V → 2.5 V up-shift operation when driving a 10 pF external load. Either a stand-alone or embedded ReBiLS design could support 500MHz operation with a 2.5 V output drive. Figure 8 illustrates 2.5 V → 0.5 V ReBiLS down-shift operation for (a) external loads of 10 pF at 100 MHz for stand-alone applications and (b) on-chip loads of 1 pF at 500 MHz for embedded applications.

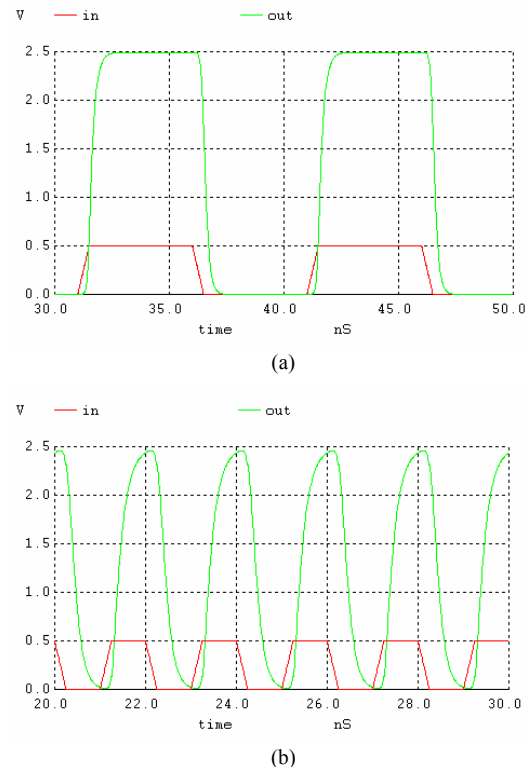


Figure 7. 0.5 V → 2.5 V up-shifting at (a) 100 MHz and (b) 500 MHz

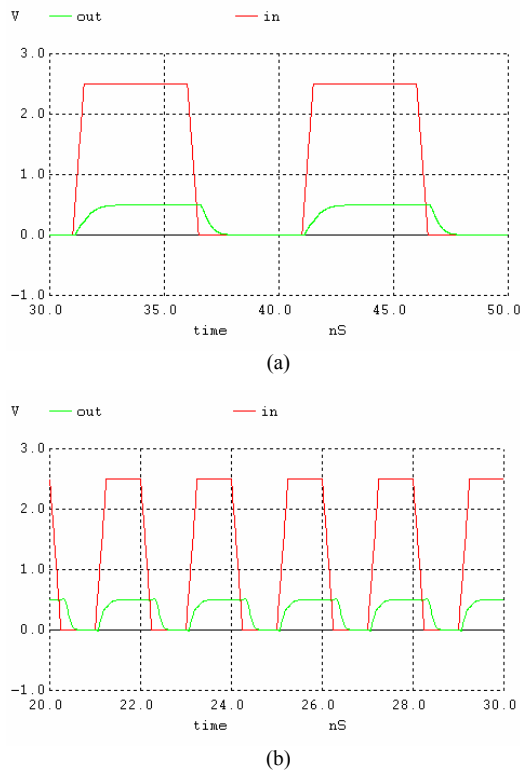


Figure 8. 2.5 V → 0.5 V down-shifting at (a) 100 MHz and (b) 500 MHz

D. ReBiLS Power Consumption

Table III provides the power consumption data for both down-shifting and up-shifting operation. The typical data is derived from the typical transistor models operating at 25 °C. The maximum data uses fast process corner transistor models operating at -40 °C. A 10 pF external load is assumed in all cases except for the down-shift to 0.5 V. Down-shifting to 0.5 V at 500 MHz would only be possible in embedded applications for which the load seen by the level shifter is the much smaller on-chip loading of low-voltage digital circuitry. The charge-discharge power of the load capacitance is a significant component of the total ReBiLS power consumption. Ultimately, embedding a ReBiLS level shifter with low-voltage logic will provide best operation by minimizing loading on the low-voltage side.

Table III
REBiLS POWER CONSUMPTION

1.8 V → 0.5 V		
	Typical (mW)	Maximum (mW)
100MHz driving 10 pF	0.53	3.23
250MHz driving 10 pF	1.00	3.55
500MHz driving 1 pF	0.68	3.29
0.5 V → 1.8 V		
	Typical (mW)	Maximum (mW)
100MHz driving 10 pF	10.42	14.59
250MHz driving 10 pF	17.08	21.35
500MHz driving 10 pF	28.67	33.64

E. Reconfigurable Operation Via Bottom Gate Control

The bottom gate control available with the ASI Flexfet™ process provides a unique advantage over typical CMOS designs. This bottom gate control allows a ReBiLS user to tradeoff operating speed (data rates, insertion delay, and transition times) with total power consumption. Figure 9, Figure 10, and Table IV provide examples of this unique bottom gate control capability in operation.

In these examples, 1.8 V ↔ 0.5 V down-shift and up-shift operations occur for two different operating modes: (a) high-speed and (b) low-power. In high-speed mode, the bottom gate voltages are $V_{nbg} = 0.5$ V, $V_{pbgh} = 1.3$ V, and $V_{pbgl} = 0.0$ V. In low-power mode, the bottom gate voltages are $V_{nbg} = 0.2$ V, $V_{pbgh} = 1.6$ V, and $V_{pbgl} = 0.3$ V. Increasing the bias across the bottom gate to source junction decreases the transistor device threshold voltages; thereby increasing speed at the expense of greater power consumption and leakage.

In low-power mode, the insertion delays and transition times are noticeably longer, but power consumption is decreased. CMOS leakage current would also be lower in low-power mode. These examples clearly demonstrate the significant advantages of bottom gate control using Flexfet™.

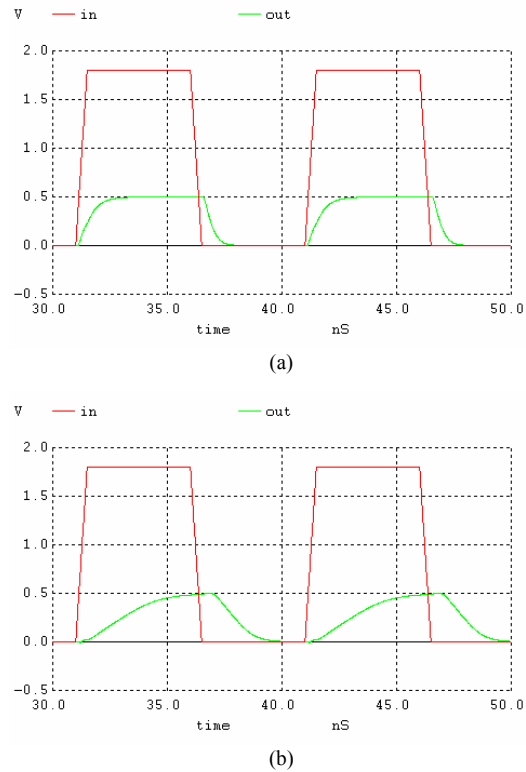


Figure 9. Reconfigurable down-shifting for (a) high-speed and (b) low-power

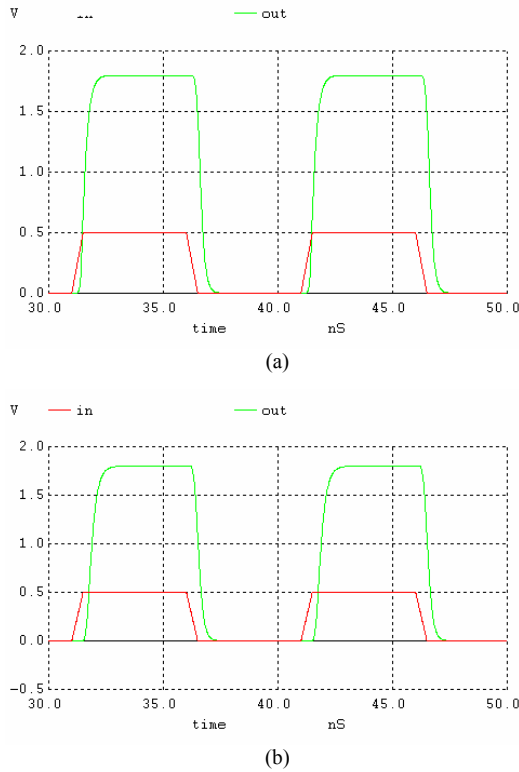


Figure 10. Reconfigurable up-shifting for (a) high-speed and (b) low-power

TABLE IV
REBiLS RECONFIGURABLE POWER SAVINGS

1.8 V \rightarrow 0.5 V		
High Speed (mW)	Low Power (mW)	Power Savings
0.53	0.31	41.4%
0.5 V \rightarrow 1.8 V		
High Speed (mW)	Low Power (mW)	Power Savings
10.42	7.59	27.2%

F. ReBiLS Operation for 3.3 V and 5.0 V

The ReBiLS design can be easily extended to support 5.0 V input and 3.3 V output with a thick-gate option for the 180nm Flexfet™ process. To interface with external circuits operating at 5.0 V (\pm 10%), there are 2 methods commonly employed within the IC industry: (1) true 5.0 V I/O and (2) 5.0V-tolerant I/O. True 5.0 V I/O devices operate with a supply voltage of 5.0 V and can both accept 5.0 V inputs and drive 5.0 V outputs. 5.0V-tolerant I/O devices operate with a supply voltage of 3.3 V (\pm 10%) and can accept 5.0 V inputs, but can only drive 3.3 V outputs as illustrated in Figure 11.

Figure 12 demonstrates that the logic levels for industry-standard 5.0 V TTL and 3.3 V LVTTTL (low-voltage TTL) are fully compatible. This allows a 3.3 V output device to drive acceptable voltage levels to interface with 5.0 V input devices.

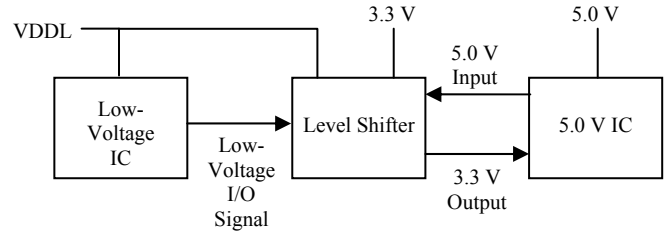


Figure 11. Application block diagram of level shifter with a 5.0V input tolerant, 3.3V output interface

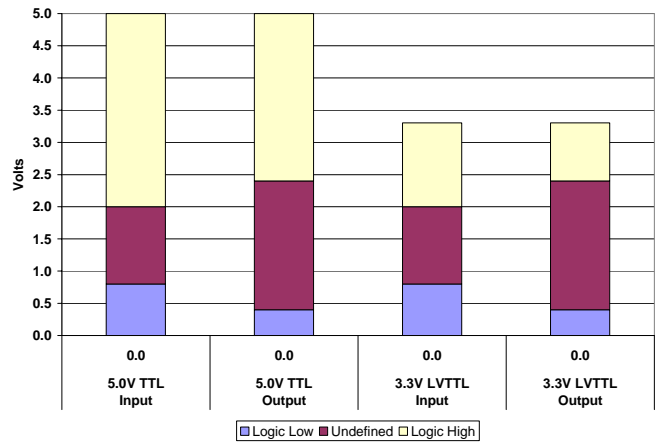


Figure 12. Comparison of 5.0 V TTL and 3.3 V low-voltage TTL logic level specifications

ASI could develop process options and circuit designs that would support true 5.0 V I/O operation. However, this would come at the expense of increased power consumption and reduced operating frequency. ASI believes the best solution is to develop process options and circuit designs that support 5.0V-tolerant input and 3.3 V output I/O operation. This would meet the needs to interface with 5.0 V and 3.3 V external devices while maximizing performance. ASI believes that developing a ReBiLS design with 5.0V-tolerant I/O would require two changes. First is addition of a high-voltage, thick-oxide option to the standard Flexfet™ 180 nm process. Second are the circuit design and layout modifications commonly employed for 5.0V-tolerant I/O designs.

IV. DISCUSSION

A. Voltage Range Limitations

Supporting a wide voltage range at either the high or low voltage side of the level shifter limits device performance. Limiting operation at one or both sides of the level shifter to ≤ 2.5 V allows for maximum performance from the basic 180 nm Flexfet™ process. Within this range, targeting 0.5 V and 1.8-2.5 V separately can provide additional performance advantages. Operation at 3.3 V requires implementation of a second oxide in the process to reliably support the higher voltages. Operation at 5.0 V for input only will require both process and design changes for reliable operation.

B. Embedded and Stand-Alone Level Shifters

Satisfying the requirements for both embedded and stand-alone level shifters with a single ReBiLS design would limit performance. Improved performance can be achieved by targeting designs separately to the embedded and stand-alone application specifications. Examples of targeted designs include:

1) Embedded ReBiLS for 0.5 V ↔ 5.0V/3.3V I/O: maximizes data rates and minimizes power consumption by limiting loads on the 0.5 V side power consumption; uses the Flexfet™ 180 nm high-voltage process option.

2) Embedded ReBiLS for 0.5 V ↔ 1.8-2.5 V: maximizes data rates and minimizes power consumption by limiting loads on the 0.5 V side power consumption; uses the standard Flexfet™ 180 nm process for increased speed and lowest manufacturing cost.

3) Stand-alone ReBiLS for 0.5 V ↔ 5.0V/3.3V I/O: supports system integration of both modern very low-voltage components with older 3.3 V and 5.0 V components; uses the Flexfet™ 180 nm high-voltage process option.

4) Stand-alone ReBiLS for 0.5 V ↔ 1.8-2.5 V: supports system integration of multi-level low voltage components; uses the standard Flexfet™ 180 nm process for increased speed and lowest manufacturing cost.

C. On-Going Activities

Single-event upset (SEU) simulations have been performed in the 180 nm Flexfet™ process. On-going simulations and test data collection will be necessary to complete ReBiLS SEE characterization. During SBIR Phase II ReBiLS prototyping will benefit from the radiation tolerant core cell development currently in progress under a contract with AFRL and the development of a radiation effects process design kit for Flexfet™.

D. Plans for Future Work

ASI has plans for additional work to complete development and manufacture of the ReBiLS designs. These activities will include:

1) Development of a high voltage, thick oxide option for the ASI 180 nm Flexfet™ process to support the design of 5.0V-input tolerant, 3.3 V output I/O cells.

2) Development of a stand-alone radiation tolerant ReBiLS integrated circuit component with two 8-channel I/O busses (total of 16 low-voltage and 16 high-voltage pins), 1.8-2.5 V I/O on the low voltage pins, 5.0V-tolerant input and 3.3 V output I/O on the high-voltage pins, and 100 MHz minimum operation with 10 pF external loads.

3) Development of an embedded radiation tolerant ReBiLS I/O cell that supports 0.5 V low-voltage operation for interface with core logic, 5.0V-tolerant input and 3.3 V output I/O pins, and 100 MHz minimum operation with 10 pF external loads.

4) Development of a 0.5 V Reed-Solomon encoder with 5.0V/3.3V ReBiLS I/O. This design will operate with 0.5 V low-voltage core logic, 5.0V-tolerant input and 3.3 V output I/O pins, and support 100 MHz minimum data rates with

10 pF external loads. This will use the ReBiLS I/O cell and transfer the existing CULPRIT Reed-Solomon encoder from a 0.35 μm bulk-CMOS process to the ASI 180 nm Flexfet™ radiation tolerant SOI process. This will demonstrate the ability to transfer IC designs from older technologies to the advanced ASI 180nm Flexfet™ radiation tolerant SOI process for use by future NASA prime contractors wishing to modernize current components or integrated circuit systems.

IV. CONCLUSION

American Semiconductor's radiation tolerant reconfigurable bi-directional level shifters (ReBiLS) can allow NASA to develop multi-level voltage systems. The ReBiLS design translates 0.5 V logic bi-directionally to 1.2 V, 1.8 V, and 2.5 V at frequencies up to 500 MHz. The radiation tolerant capability of the ReBiLS design is derived from the Flexfet™ technology which has demonstrated total ionizing dose (TID) tolerance in excess of 1 Mrad. Control of the bottom gate voltages allows reconfiguration to tradeoff power consumption and operating speed. ReBiLS designs that support voltage translation to 3.3 V and 5.0 V can be achieved with process and circuit modification. A stand-alone ReBiLS device will allow system designers to provide efficient bi-directional communication between components operating at different voltages. A ReBiLS standard cell, optimized for new embedded applications, will permit single chip integration of low-voltage, low-power core logic with high-voltage I/Os.

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