

Flexfet CMOS for ULP Electronics

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Abstract: Flexfet™ independently-double-gated (IDG) CMOS in double-gate (DG) 0.5V mode has near ideal 64 mV/decade subthreshold slope and I_{on}/I_{off} ratios of 10^5 . In IDG mode, Flexfet provides dynamic V_t control. Dynamic V_t , sub-Volt capability and near ideal sub-threshold slope are shown to provide a basis for superior OPS/Watt capability in ULP applications.

Keywords: double gate; MOSFET; JFET; Flexfet; semiconductor manufacture; FinFET.

Introduction

Double-gate (DG) MOSFETS have been presented as solutions to transistor scaling problems due to their excellent short-channel effect (SCE) immunity. Also, the improved subthreshold slope of DG devices can provide operation at lower supply voltages while still providing sufficient I_{on}/I_{off} ratios for operation of logic and memories. Independently-double-gated (IDG) FinFETs were reported as FT-FinFETs for flexibly controlling threshold voltage by Liu in 2003 [1]. However, DG and IDG FinFETs face several challenges limiting commercial fabrication [2-3]. This paper presents experimental results for both NMOS and PMOS IDG FETs (Flexfet). Planar Flexfet transistors provide a manufacturing friendly alternative to FinFET devices. Flexfet allows optimization for ultra-low-power (ULP) circuits and has been evaluated for scaling to 32nm [4].

Basic Operation

A Flexfet transistor is a four terminal device composed of a metal-gate, fully depleted, SOI MOSFET in parallel with a self-aligned JFET sharing a common source and drain (Figure 1) [5]. Flexfet is a true double-gate transistor in that (1) both the top and bottom gates provide transistor operation and (2) the operation of the gates is coupled such that the top gate operation affects the bottom gate operation and vice versa.

There are two primary schemes for connecting the Flexfet transistor: double-gated (DG) or independently-double-gated (IDG). In DG operation, the top and bottom gates are electrically connected as illustrated in Figure 2 to create a 3-terminal transistor. In IDG operation, the top and bottom gates are electrically isolated as illustrated in Figure 3, and typically, the bottom gate is used to dynamically adjust the threshold voltage (V_t) of the transistor as seen from the top gate. IDG transistors such as Flexfet are also sometimes referred to as a Multiple Independent Gate FETs, or MIGFETs. Flexfet supports integration of both DG and IDG transistors within a single design and without any

additional process steps. The connections are made during routing to both the top and bottom gates just as to the source and drains.

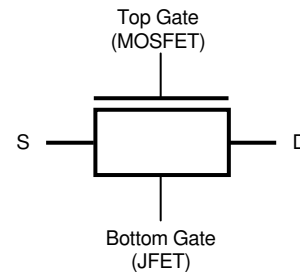


Figure 1. Flexfet schematic representation

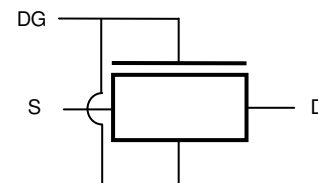


Figure 2. Flexfet Connections for Double-Gated (DG) Operation

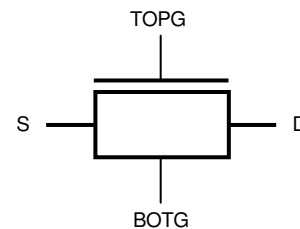


Figure 3. Flexfet Connections for Independently-Double-Gated (IDG) Operation

Fabrication Process

Within the semiconductor industry, FinFET is the most well known double-gate transistor technology. Whereas a typical MOSFET transistor is planar, the FinFET is manufactured vertically. The vertical FinFET device with two MOSFET gates has been heavily investigated over the past decade but still faces many hurdles to significant industry adoption due to the challenges of integrating a 3-D structure using non-standard process technology. The difficulties of fabricating the FinFET DG FET include the variability of the fin (silicon channel) thickness, the inability to adjust the transistor width, and the integration scheme for the source/drain of complementary NMOS FETs and PMOS FETs on the same wafer for the gate-last process [2-3].

Flexfet employs a very efficient sub-litho, planar fabrication process (unlike FinFET) that includes raised source and drain, gate-last metal top gate, and only 10 masking steps to build Flexfet CMOS circuits through the first metal layer (MM1). Figure 4 illustrates a cross-section of the planar Flexfet transistor across the transistor length. In this figure, all 4 transistor nodes are visible: top gate (TG), bottom gate (BG), source (S), and drain (D). In addition, the buried oxide (BOX), local interconnect layer (M0), and isolation (STI) are shown.

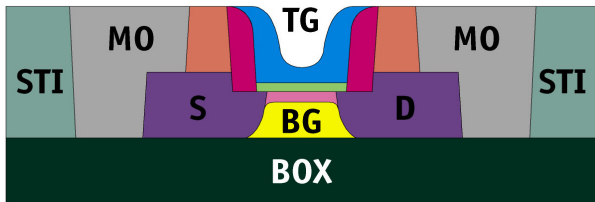


Figure 4. Flexfet cross-section

The starting material is p-type SOI. Shallow SD implants are followed by deposition of a nitride pad. Isolation and gate trenches are simultaneously etched through the nitride and into the SOI to separate the source from the drain. A bottom gate (BG) mask is used to protect the channel regions while completing the isolation etch down to the BOX. This is followed by creation of oxide/nitride spacers.

The spacer-lined sub-litho gate trench is used to self-align a high concentration bottom gate implant near the BOX interface to form the JFET bottom gates and set the thickness of the fully depleted channel. Thermal gate oxidation followed by mid-gap metal deposition is then applied. Top gate mask and CMP define the top gate (TG) to form the MOSFETs. This gate-last process supports integration of high-k gate dielectrics and a wide variety of alternative metal gates. The four terminals of the IDG transistors are contacted with local interconnect and then standard multilayer processing is used to complete the metal interconnect fabrication. A SEM photo of a Flexfet transistor prior to STI deposition is shown in Figure 5.

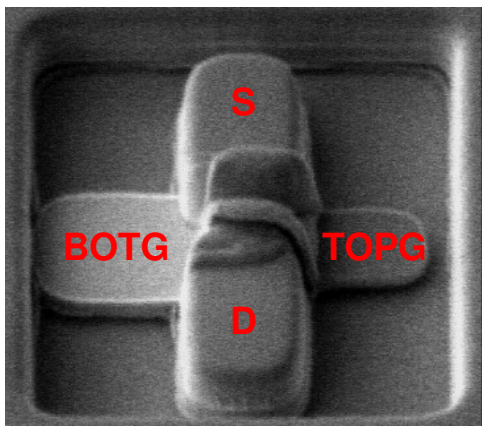


Figure 5. SEM photo of single 0.18 μm independently-double-gated (IDG) Flexfet transistor.

Experimental Data

All data presented is for Flexfet transistors with physical gate length of 0.18 μm with the source grounded. Figure 6 shows the I_d - V_{dg} curve of a Flexfet NMOS transistor operating in double-gated (DG) mode as a three terminal device with the top and bottom gates electrically connected. The theoretical subthreshold slope of a double-gated transistor is 60 mV/decade. The subthreshold slope of the DG NMOS Flexfet transistor is 64 mV/decade. Figure 7 provides the I_d - V_{dg} curve for the Flexfet PMOS transistor demonstrating a subthreshold slope of 67 mV/decade.

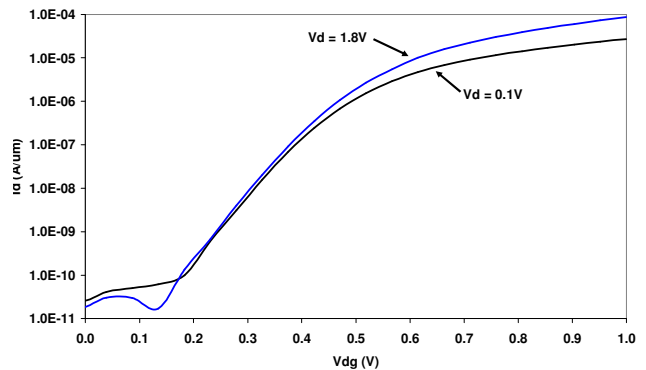


Figure 6. Double-Gated Flexfet NMOS 0.18 μm I_d - V_{dg} showing near ideal double-gated subthreshold slope of 64 mV/dec.

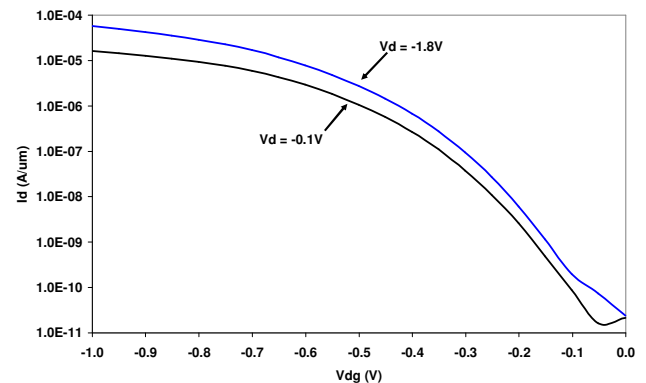


Figure 7. Double-Gated Flexfet PMOS 0.18 μm I_d - V_{dg} showing near ideal double-gated subthreshold slope of 67 mV/dec.

In Figure 8, the Flexfet NMOS device is operating as a four terminal independently-double-gated (IDG) transistor. The bottom gate bias adjusts the threshold voltage (V_t) of the I_d - V_{topg} curve. As the bottom gate voltage is increased, the threshold voltage of the Flexfet transistor decreases. The noise floor of the test setup limited measurement of current below 100pA. The variation of V_t with the bottom gate voltage is illustrated in the graph of Figure 9. Figure 10 demonstrates that other than the dramatic shift in V_t , the basic Flexfet transistor operation is relatively unchanged by the adjustment of the bottom gate voltage. The transistor continues to exhibit a good ratio of I_{on} to I_{off} and excellent control of drain induced barrier level (DIBL).

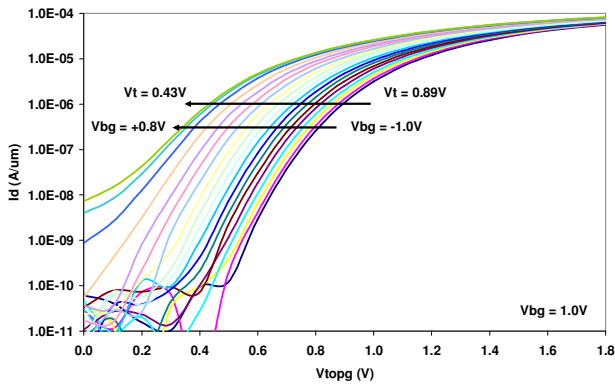


Figure 8. IDG Flexfet NMOS 0.18µm I_d - V_{topg} as a function of V_{botg} demonstrating 460mV of V_t shift.

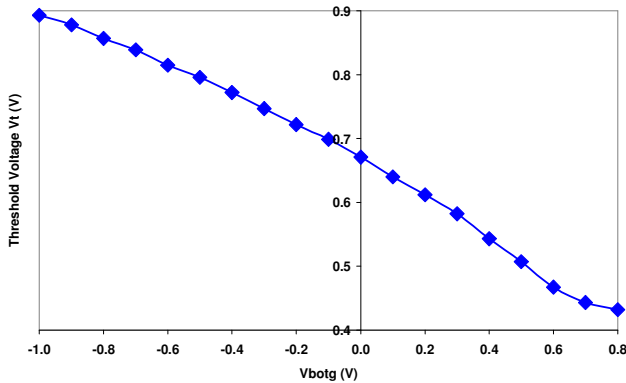


Figure 9. IDG Flexfet NMOS 0.18µm threshold voltage (V_t) variation as a function of the bottom gate voltage (V_{botg}).

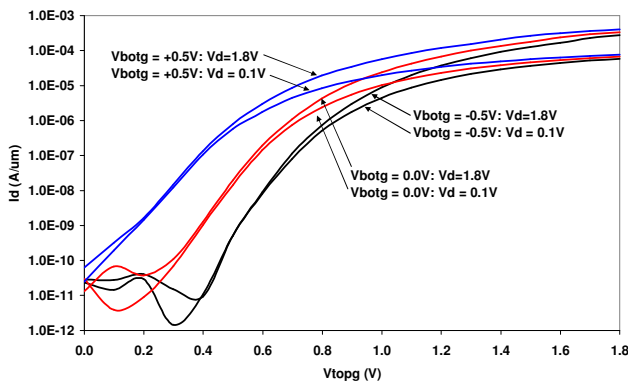


Figure 10. IDG Flexfet NMOS 0.18µm I_d - V_{topg} as a function of V_{botg} in both linear ($V_d = 0.1V$) and saturation ($V_d = 1.8V$) demonstrating limited DIBL.

Figures 11-13 provide the complementary set of curves for the Flexfet PMOS transistor. The data demonstrates that the Flexfet process supports complementary NMOS and PMOS transistors suitable for integrated circuit design applications.

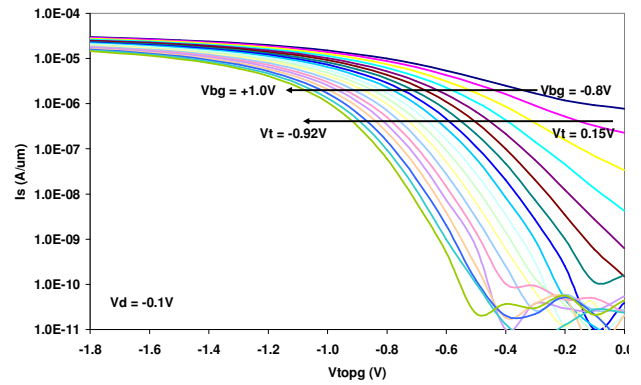


Figure 11. IDG Flexfet PMOS 0.18µm I_d - V_{topg} as a function of V_{botg} demonstrating 770mV of V_t shift.

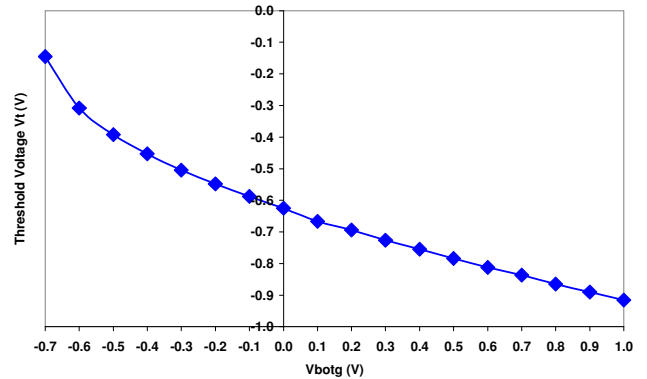


Figure 12. IDG Flexfet PMOS 0.18µm threshold voltage (V_t) variation as a function of the bottom gate voltage (V_{botg}).

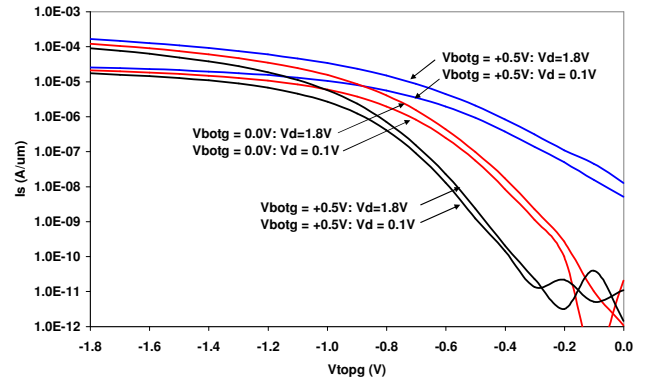


Figure 13. IDG Flexfet PMOS 0.18µm I_d - V_{topg} as a function of V_{botg} in both linear ($V_d = -0.1V$) and saturation ($V_d = -1.8V$) demonstrating limited DIBL.

Figures 14 and 15 (on the following page) provide the Flexfet I_d - V_d set of curves for two different set of bottom gate bias conditions: $V_{botg} = +0.5$ and $V_{botg} = -0.5V$. On this linear scale the variation in transistor drive current with bottom gate bias is readily apparent. Changing the transistor threshold voltage results in a subsequent change in the transistor drive current.

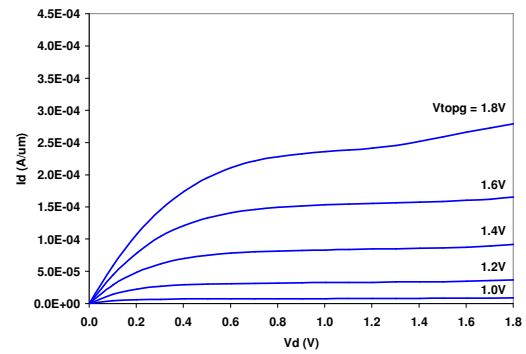
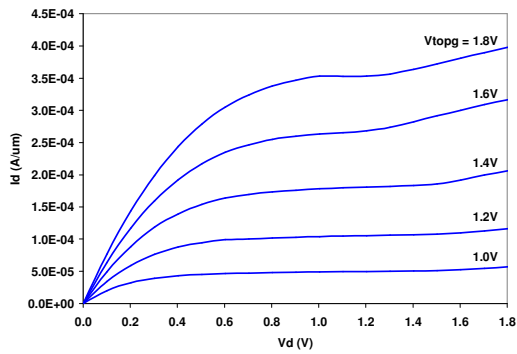


Figure 14. IDG Flexfet NMOS Id-Vd curves for $V_{botg} = +0.5V$ (left) and $V_{botg} = -0.5V$ (right).

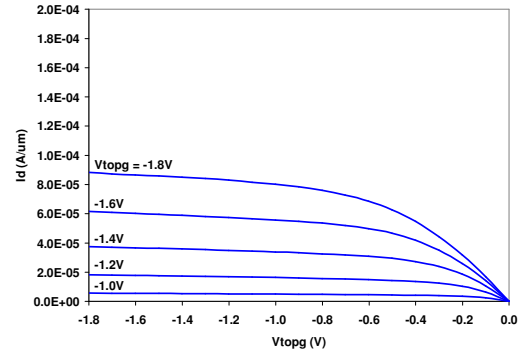
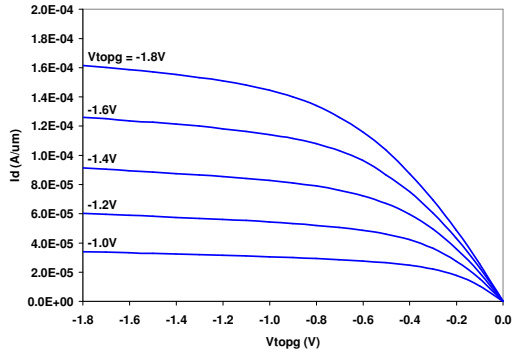


Figure 15. IDG Flexfet PMOS Id-Vd curves for $V_{botg} = -0.5V$ (left) and $V_{botg} = +0.5V$ (right).

Applications

Employing the IDG capability of Flexfet allows dynamic reconfiguration of circuit performance relative to operating conditions. This allows optimization of both performance and power consumption for ULP applications. The bottom gate potentials can be adjusted to provide higher threshold voltages and thus lower off currents when the circuit is idle. Conversely, the threshold voltages can be minimized to increase the operating frequency of the circuit when highest performance is required. Other applications of Flexfet's IDG capability include countering process variation and compensating for threshold voltage shifts caused by radiation damage.

Combining IDG and DG transistors within a circuit can allow further optimization of circuit performance for ULP applications. Dynamic V_t adjustment plus steeper subthreshold slope may allow dramatic scaling of the supply voltage without suffering from the typical limitations of low performance or high leakage.

Conclusions

Experimental data has demonstrated that the Flexfet process enables manufacture of complementary NMOS and PMOS transistors that can be connected in either double-gated (DG) or independently-double-gated (IDG) configurations. The planar Flexfet process is significantly easier to manufacture than the non-planar FinFET double-gated transistors and thus provides an alternative scaling path to solve many of the deep sub-micron challenges

facing the semiconductor industry. Ultra-low-power applications could benefit from both dynamic threshold voltage control and steep subthreshold slope for improved power efficiencies, as measured in operations per second per Watt (OPS/Watt).

Acknowledgements

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