Design of a 32nm Independently-Double-Gated FlexFET SOI Transistor

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***Abstract*—Considerable recent research has focused on developing vertical FinFET-type double-gated CMOS devices. Planar independently-double-gated FlexFET CMOS transistors have recently been reported, exhibiting strong dynamic threshold voltage control. The FlexFET device design utilizes a mid-gap metal top gate self-aligned to an implanted JFET bottom gate. A simple analytical dynamic threshold model is developed in this work and verified by extensive device simulation. Optimization of the top gate oxide thickness, silicon thickness, and gate work functions for a 32nm node FlexFET CMOS technology is achieved by device simulation using SILVACO. Ideal dynamic threshold control of this 32nm device is achieved with relatively thick 11nm silicon and 4nm gate oxide thicknesses.**

***Index Terms*—CMOS, FlexFET, independent double gated transistors, short channel effect, SOI.**

I. Introduction

MOSFET technology has advanced from bulk MOSFETs to partially depleted SOI MOSFETs, to DTMOS, to fully depleted SOI MOSFETs, to double gate SOI MOSFETs, to triple gate MOSFETs and Surround gates as shown in Figure 1.

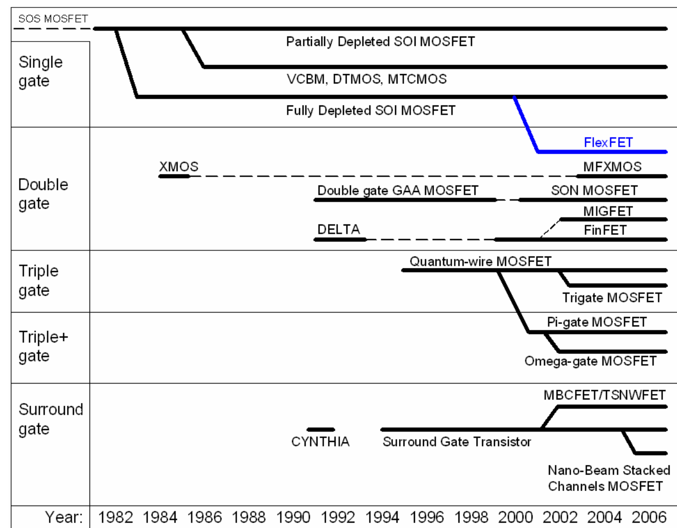

Fig. 1 SOI and Multigate MOSFETs "Family Tree" [1]

Double gated MOSFETs allow for a reduction in short channel effects and continued device scaling. Independent double gate (IDG) SOI MOSFETs allow for dynamic threshold voltage control. One IDG SOI MOSFET was derived from the double gate FinFET, and called the Multiple Independent Gate FET (MIGFET) [2]. The MIGFET has independent gates to the left and right of the silicon channel fin which can be biased to dynamically control the threshold voltage. FlexFET is another IDG SOI MOSFET with independent top and bottom gates [3]. It was derived from the single gate fully depleted SOI MOSFET. The bottom gate of FlexFET can also be biased for dynamic control of the threshold voltage. FlexFET is a SOI IDG-CMOS technology with a damascene metal top gate and an implanted JFET bottom gate that are self-aligned in a gate trench, as shown in Fig. 2.

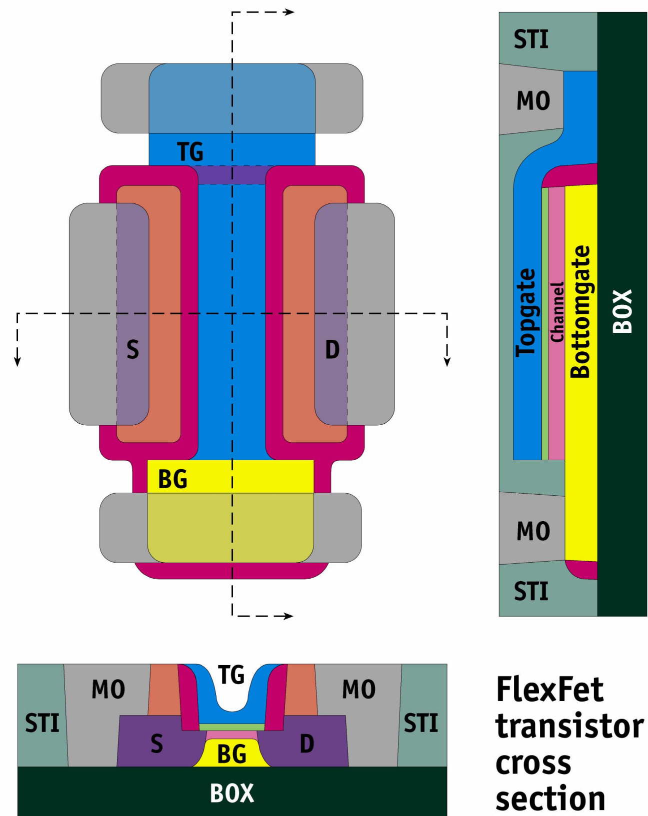

Fig. 2 FlexFET Transistor top view (top left), cross sectional lines on the top view point toward the appropriate cross sectional view. [3]

The independent top and bottom gates are contacted at opposite sides of the channel by a local interconnect that is embedded in the isolation region between devices. This results in compact, planar connections to all four transistor terminals as shown in Fig. 3. Individual transistors can be connected in single gate (SG), double gate (DG), or independent double gate (IDG) mode, as desired by the circuit designer. The MIGFET and the FlexFET are the only two IDG SOI MOSFETs in production today by Freescale Semiconductor and American Semiconductor, respectively.

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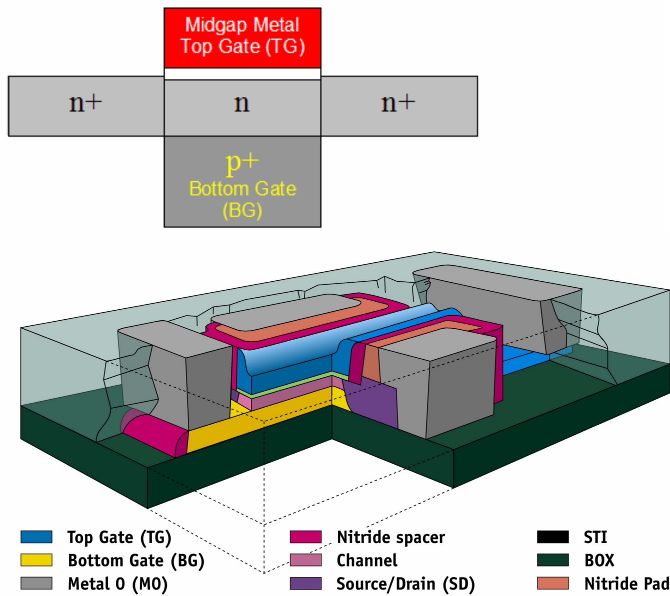

Fig. 3 Side view and 3D view of NMOS FlexFET [3]

In addition to the single and double gate SOI MOSFETs, triple gate and surrounding gate MOSFETs also exist. The surrounding gate is the "structure that theoretically offers the best possible control of the channel region by the gate."[1] An overview of the all the different MOSFET gate structures is shown below in Figure 4.

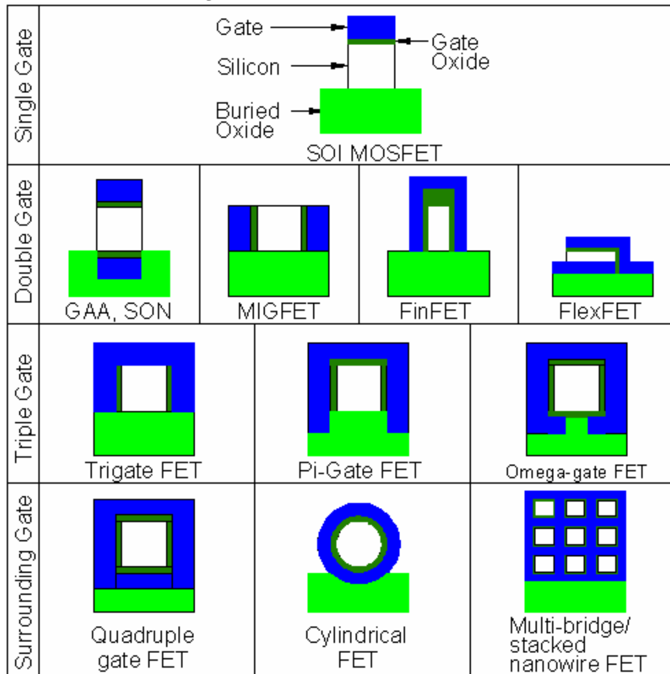

Fig. 4 Different gate structure with current going into the page.

This paper will focus on optimization of the top gate oxide thickness, silicon thickness, and gate work functions for a 32nm node FlexFET CMOS technology by device simulation using SILVACO.

II. IDG SOI FLEXFET BEHAVIOR

IDG SOI FlexFETs allow for dynamic control of the top gate threshold voltage by applied voltage to the bottom gate when they are fully depleted. When partially depleted, the top and bottom gates are decoupled and their voltages do not have an effect on each other. When fully depleted, there are three regions which the back gate can operate as shown in Fig. 5.

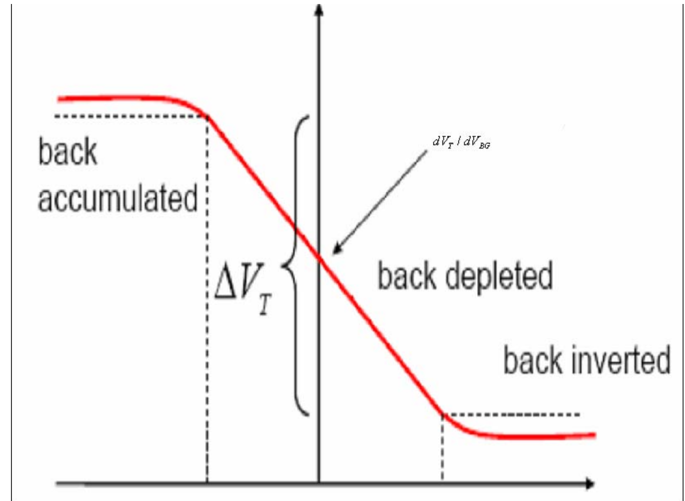

Fig. 5 Threshold voltage vs. bottom gate voltage characteristics

It is not desirable to operate in the back accumulated or back inverted region because they are two extremes of net threshold voltage swings. The back inverted region does not allow the device to turn off and the back accumulated does not allow for the device to turn on. The mode of operation we are interested in is the back depleted region where the slope of the curve is the control factor (f). The ideal control factor is 1 which means if the bias of the back gate is 1V it changes the threshold voltage by 1V as well.

The FlexFET allows the bottom gate to be biased positive for applications requiring high performance and biased negative for applications needing lower power consumption. Fig. 6 shows the tradeoffs between power and speed.

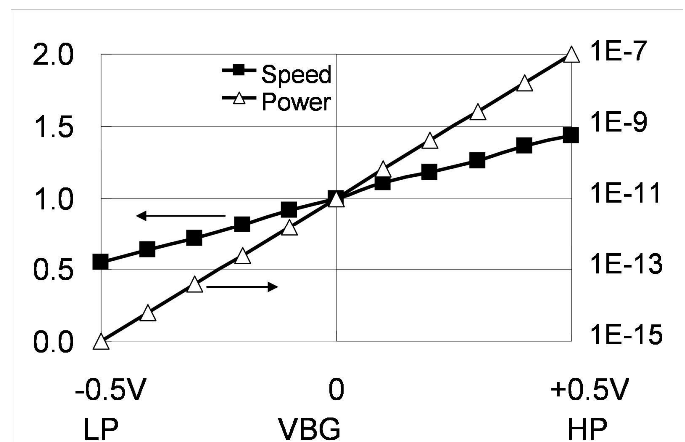

Fig. 6 Speed and power effects vs. bottom gate voltage bias [4]

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III. Design Simulation Results

Planar independently-double-gated FlexFET CMOS transistors have recently been reported, exhibiting strong dynamic threshold voltage control [4-6]. The FlexFET threshold voltage and degree of bottom gate threshold control are dependent on the silicon thickness, oxide thickness, channel length, and top & bottom gate work functions as shown in (1) and (2).

$$V_T = V_{FBTG} + (1+f)\phi_{ST} - f(V_{BG} - V_{FBBG}) \qquad (1)$$

V_T = Threshold voltage

V_{FBTG} = Top gate work function difference

V_{FBBG} = Bottom gate work function difference

ϕ_{ST} = Top gate surface potential

f = Control factor

Since the device is fully-depleted and FlexFET has no bottom gate oxide, the bottom gate control factor simplifies to (2).

$$f = \frac{C_{SI}}{C_{TOX}} = \frac{3t_{OX}}{t_{SI}} \qquad (2)$$

t_{OX} = Top gate oxide thickness

t_{SI} = Silicon thickness

Ideal volt per volt bottom gate threshold control implies f=1, so we must have the silicon thickness equal to three times the top gate oxide thickness. Both the threshold and bottom gate control factor vary inversely with the silicon thickness but linearly with the top gate oxide thickness, as seen in the Silvaco ATLAS device simulation results in Figs. 7-8.

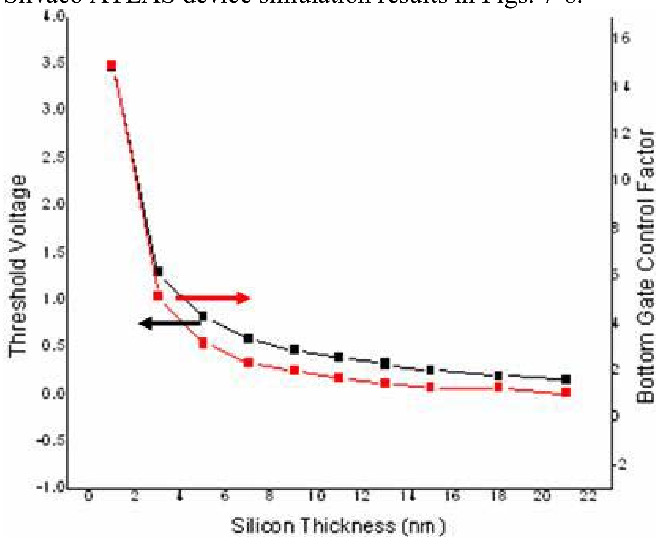

Fig. 7 FlexFET threshold and bottom gate control vs. silicon thickness

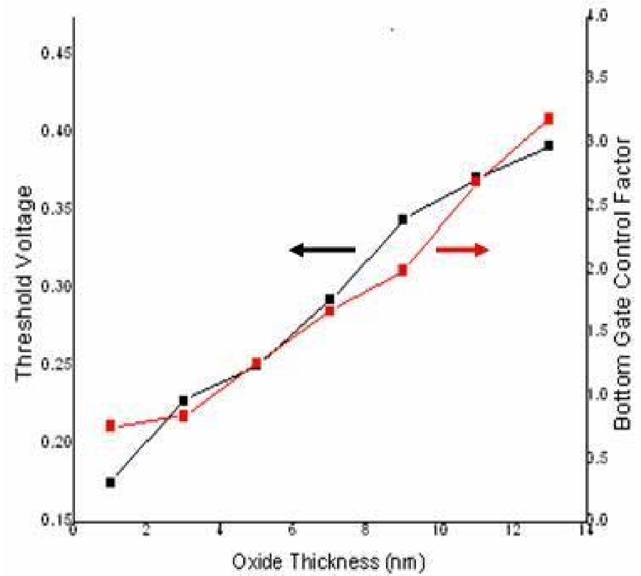

Fig. 8 FlexFET threshold and bottom gate control vs. top gate oxide thickness

The SILVACO simulation results show that f stays constant near unity for mid-gap and below gate work functions, but rolls off rapidly as either gate work function approaches the conduction band (Figs. 9-10).

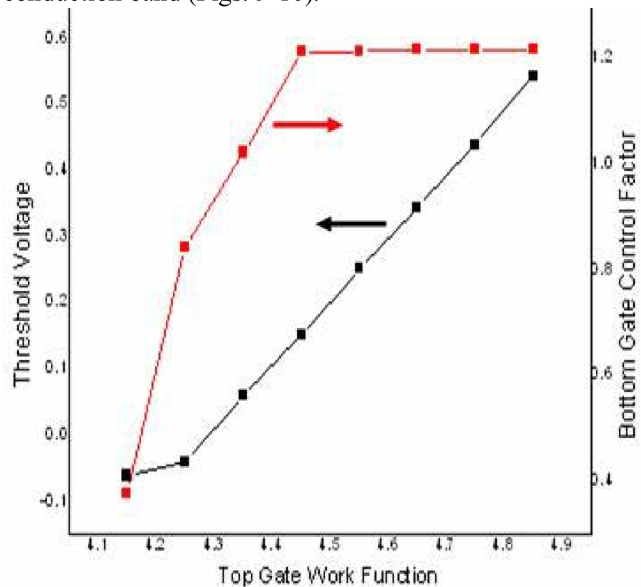

Fig. 9 FlexFET threshold and bottom gate control vs. top gate work function

This is because the device is no longer fully-depleted with these work functions. The threshold varies as expected with top and bottom gate work functions. Because there is no bottom gate oxide in FlexFET, the effect of the bottom gate work function on the threshold voltage is strong.

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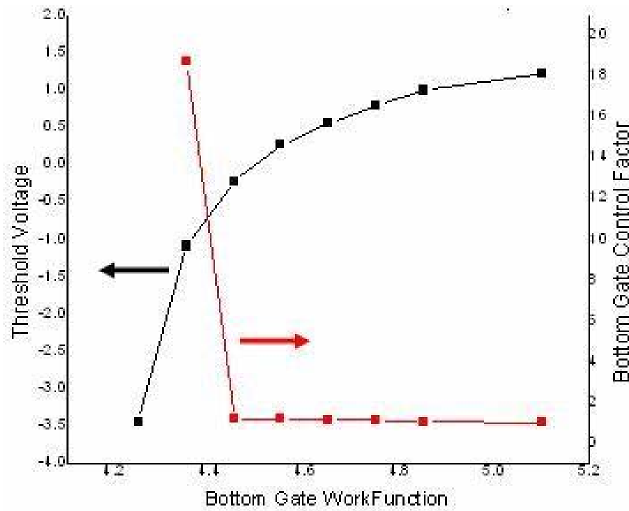

Fig. 10 FlexFET threshold and bottom gate control vs. bottom gate work function

The short channel effect (SCE) simulations show that when the threshold rolls off at short channel lengths, the bottom gate control (f) increases simultaneously. This implies that bottom gate bias can be used very effectively to mitigate SCE roll off in FlexFET transistors, where for instance a 0.5V bottom gate bias can shift the threshold by +1.0V, thus shifting the threshold of the 32nm device from -0.7V to +0.3V, as shown in Fig. 11.

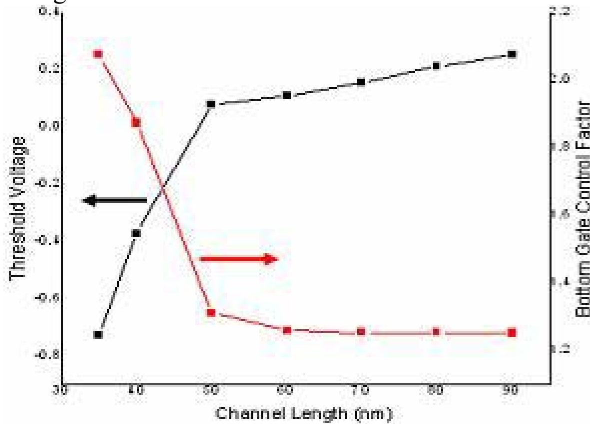

Fig. 11 FlexFET threshold and bottom gate control vs. channel length

IV. 32 NM OPTIMAL DEVICE DESIGN

We considered the optimal design of a 32nm channel length FlexFET NMOS by varying the thickness of the silicon and oxide while the top gate work function was pinned at TiN and the bottom gate work function was pinned at the P+ valence band edge. The conditions of ideal f=1 bottom gate threshold control and adequate SCE roll off were maintained, resulting in a design curve of appropriate silicon and top gate oxide thicknesses, as shown in Fig. 12.

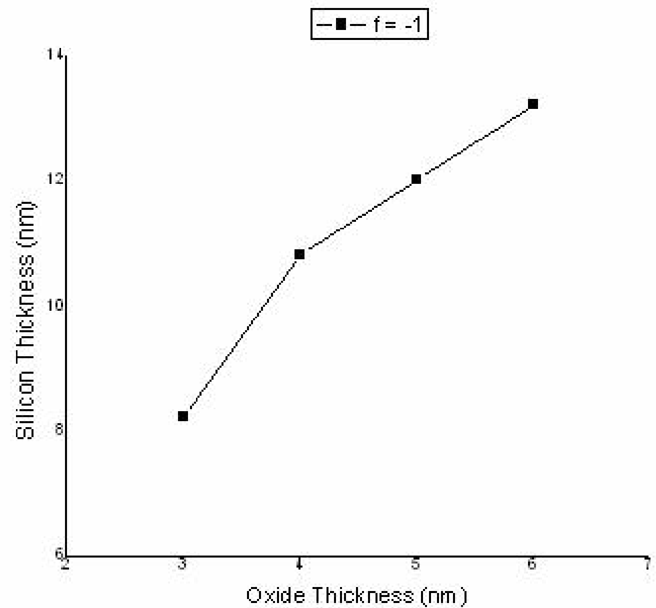

Fig. 8 Optimal silicon and oxide thickness for a 32nm FlexFET

The combination of top gate oxide thickness equal to four nanometers and silicon thickness equal to eleven nanometers was found to meet all optimal design criteria.

V. CONCLUSIONS

Using device simulation, we have optimized the design a 32nm node FlexFET NMOS for ideal bottom gate threshold control.

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