Ultra-Low-Power, High-Performance, Dynamic-Threshold Digital Circuits in the FlexFET Independently-Double-Gated SOI CMOS Technology

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Introduction

The ITRS roadmap projects that double-gated transistors will be needed in the future, in order to scale CMOS to the 45nm node. However, flexible, dynamic threshold control is possible now with existing independently-double-gated (IDG) CMOS technologies, and is highly desirable for ultra-low-power (ULP) SoC designs at the 180nm, 130nm, and 90nm nodes [1]. By varying the bottom gate voltage of the FlexFET IDG MOSFET from -0.5V to +0.5V, standby power can be dynamically changed over **ten orders** of magnitude, while the transistor/circuit performance can be changed by 70%. Minimally sized transistors may be used to achieve ULP in standby, while dynamic Vt adjustment is used to achieve high-performance when active. This paper demonstrates IDG FlexFET CMOS in static CMOS ring oscillators, while the advantages of applying IDG-CMOS to dynamic domino CMOS logic circuits have recently been shown as well [1]. IDG-CMOS has also recently been applied to several exciting new analog/MS/RF circuit applications, such as a single transistor mixer [5]

Device Description

FlexFET is a new SOI IDG-CMOS technology [2-4] that features a gate trench etched through thick SD regions into which an implanted JFET bottom gate and mid-gap TiN MOS topgate are self-aligned, as shown in Fig. 1. The independent top and bottom gates are contacted at opposite sides of the channel by a damascene tungsten local interconnect (LI) that is embedded in the isolation region between devices. This results in compact, planar connections to all four transistor terminals. Individual transistors can be connected as single gate (SG), double gate (DG), or (IDG) as required. Fig. 2 shows an SEM topview of an IDG inverter ring oscillator (taken after LI mask). All NMOS bottomgates are connected to NBG and all PMOS bottomgates are connected to PBG. Fig. 4 shows the schematics of the three inverter types investigated. The SG and IDG types can both operate to VDD=2.5V, while the DG type can only operate to VDD=1.0V. Fig. 3 shows that a measured bottomgate threshold control of >0.85V/V was achieved. This high degree of control means that only a small bottomgate voltage range of -0.5V to +0.5V is required to achieve the desired ultra-low-power and high performance targets. No additional area was required to make the bottomgate contacts.

Process Description

The FlexFET process uses a relatively thick 200nm SIMOX SOI layer into which SD's are implanted. Gate trenches are then etched through the SD's. The channel thickness is set by the energy of the bottomgate implant into the bottom of the gate trench, not by the SOI thickness. A raised SD structure is achieved without any epi growth thermal budget. FlexFET is a "gate-last" process, allowing high-K or ferroelectric gate dielectrics and metal topgates to be deposited and planarized into the gate trench, thus avoiding any damaging plasma gate etches or subsequent high-temperature processing. Ultrashallow SDE's are formed by disposable doped glass sidewall spacers. PECVD PSG & BSG conformal spacers with 5% dopant concentration were created on the gate trench sidewalls, used to drive in the SDE's, and then removed and replaced by nitride spacers. These nitride spacers permit 180nm channels to be created with relaxed 350nm lithography. A 4.5nm oxynitride and a 30nm TiN layer form the topgate stack. Only 8 masks were used through M1. The recessed channel & bottomgate structure maintains an ultra-thin 20nm channel while allowing 200nm thick SD's for lower SD series resistance. These unique device structural features make the FlexFET transistor highly scalable.

Results & Discussion

Fig. 5 shows the IDG-CMOS propagation delay as a function of both NBG and PBG. The slowest condition (44ps) is for both bottomgates "off" at -0.5V, while the fastest condition (26ps) is for both bottomgates "on" at +0.5V. The table in Fig. 6 shows that the threshold voltage can be varied by 0.85V, resulting in the standby current reduced to 10^{-16}A/um at -0.5V, while the drive current is increased to 850uA/um at +0.5V. Essentially all static & dynamic digital circuits, as well as analog/MS/RF circuits can benefit from IDG operation.

References

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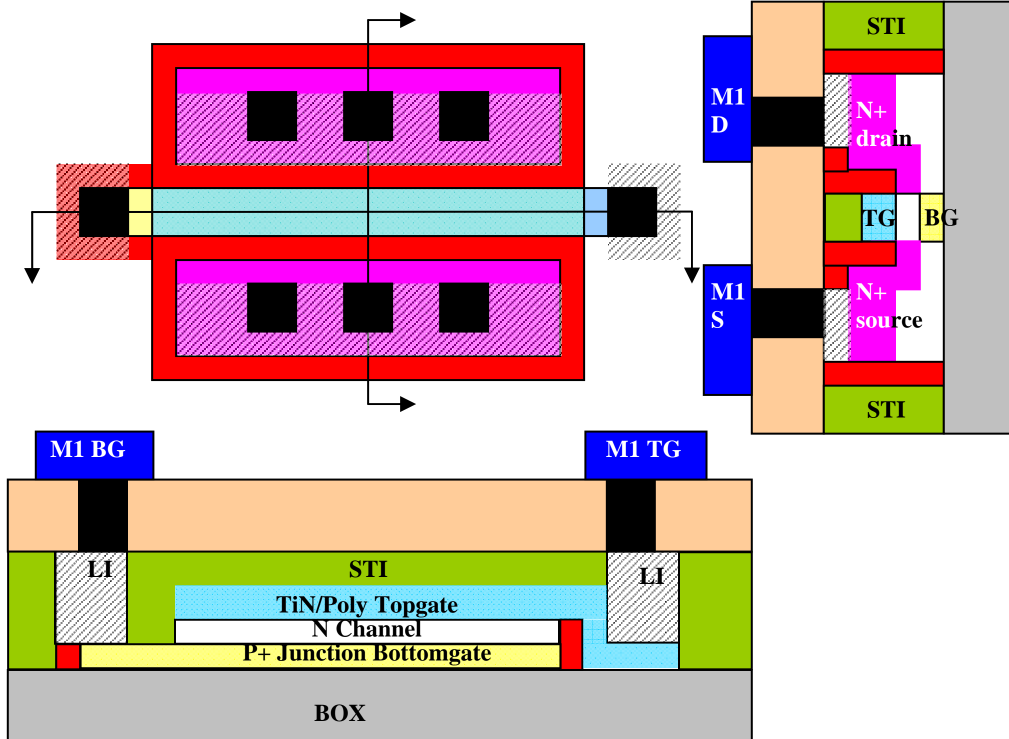

Fig. 1 FlexFET NMOS Top View and X & Y Section Drawings

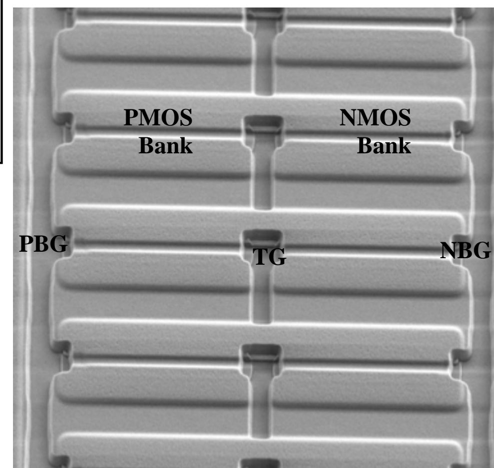

Fig. 2 FlexFET IDG-CMOS Inverter Oscillator SEM

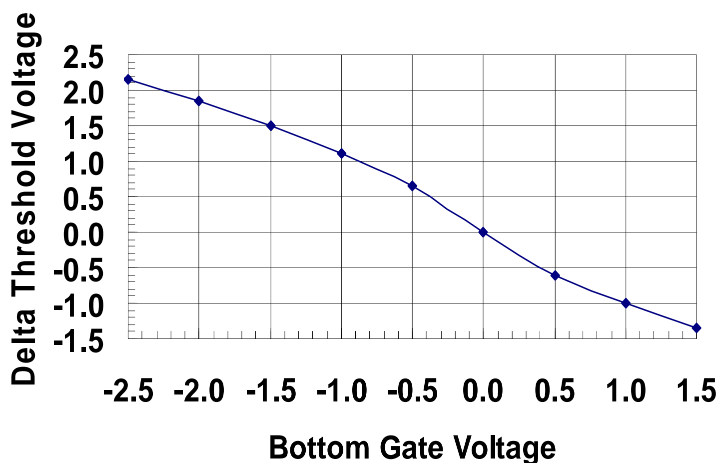

Fig. 3 Measured NMOS Vt shift vs. BG Voltage, showing >0.85V/V

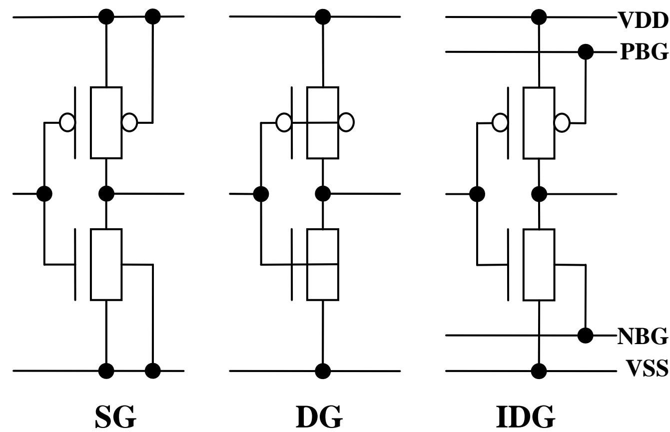

Fig. 4 SG, DG, IDG Ring Oscillator Schematics

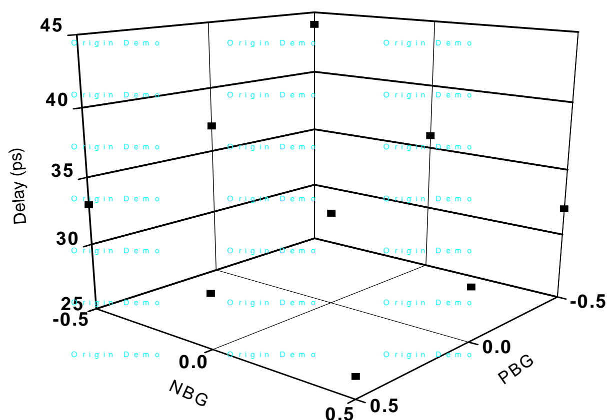

Fig. 5 IDG-CMOS Propagation Delay vs. BG Voltages

		Slow ULP	Nominal	Fast HP
NBG & PBG	V	-0.5	0	+0.5
VT	V	0.85	0.425	0
Ioff	uA/um	1.0E-10	1.0E-05	1
Pstandby	uW/um	2.5E-10	2.5E-05	2.5
Ion (NMOS)	uA/um	520	700	850
Pactive	uW/um	191	263	323
Prop Delay	psec	44	32	26
PDP	fJ/um	8.4	8.4	8.4

Fig. 6 180nm FlexFET IDG-SOI CMOS Performance Table